

An Electronics Division Retrospective (1952-2002) and Future Opportunities in the Twenty-First Century

To cite this article: Howard R. Huff 2002 *J. Electrochem. Soc.* **149** S35

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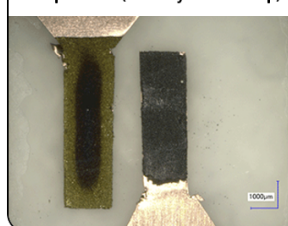
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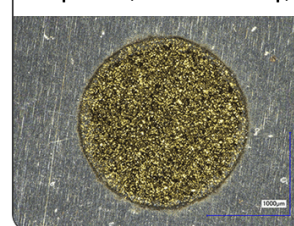
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An ECS Centennial Series Article

An Electronics Division Retrospective (1952-2002) and Future Opportunities in the Twenty-First Century

Howard R. Huff*

International SEMATECH, Austin, Texas 78741, USA

The emergence of crystalline silicon and silicon-based materials such as silicon-germanium as the premier materials and the personnel driving the integrated circuit (IC) microelectronics revolution will be reviewed. The major threshold events from the 1940s through the mid-1960s, presaging the onset of the large scale integration microelectronics era, will be highlighted. The major silicon material challenges such as dislocation-free single-crystal growth, plastic deformation, the point-defect dilemma, gettering, oxygen in silicon, carrier lifetime, and controlled point-defects in the silicon crystal during the evolution of silicon microelectronics from large scale integration through the very large scale integration era in the 1970s and the 1980s into the ultralarge scale integration era of the 1990s will then be reviewed. Opportunities in epitaxy, wafer cleaning, silicon-on-insulator, silicon-germanium, IC scaling and potential changes in device configuration and IC architecture in the evolution towards the 64 Gbit DRAM and 9 G transistor high-performance MPU logic era in 2016 (per the 2001 edition of the International Technology Roadmap for Semiconductors) will be discussed in the context of silicon-based microelectronics. The complementary role of compound semiconductors, nanoelectronics and the continuing initiative to obtain an optoelectronic system compatible with silicon will also be discussed. Finally, nonsilicon materials and device configurations will briefly be noted.

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Available electronically April 11, 2002.

Status-1952

The computer and communications age has catapulted electronics to its current status as the dominant global industry. Indeed, we are in the midst of a revolution brought about by the availability of inexpensive information acquisition, manipulation, and distribution systems. Exploitation of electron and hole conduction in silicon has resulted in electronic memory and logic circuits such as the dynamic random access memory (DRAM) and microprocessor. Control of the interaction of photons with compound semiconductors has resulted in optical devices such as the laser and optical fiber networks. This revolution has been and will continue to be dependent on our ability to control electronic and photonic material processing techniques for the manufacture of useful devices, circuits and systems. The preparation and detailed processing sequence of a material from crystal growth through device and circuit fabrication determines the microstructure and, therefore, the electronic properties of the material and resulting device and circuit performance, yield, and reliability. Electronic materials include semiconductors, dielectrics, magnetics, piezoelectrics, optoelectronic materials, and optical fibers which may be utilized in crystalline, polycrystalline, or amorphous form. Materials are indeed the *sine qua non* of electronic and optical devices and circuits.

An extensive list of relevant citations through 1997 is noted in Ref. 1, a small number of which will be referred to in the course of this review. A review from 2001 contains an additional set of updated references.² Finally, a complementary set of relevant references is also cited.^{3,4} Of course, only a small subset of the Electronics Division (ED) thrust could possibly be included in this brief review. Needless to say, retrospective assessments are very subjective and projections are the result of less than prescient skill, so this article should, perhaps, be pursued cautiously. ED initiatives very relevant to integrated circuit (IC) fabrication, yet not significantly covered, moreover, include chemical vapor deposition, the Si/SiO₂ interface, ion implantation, low-k and high-k dielectric materials, metallization, patterning science and technology, plasma etching, analytical and diagnostic techniques, process modeling and control, and packaging, as well as diamond and diamond-like films, high-temperature superconductors, sensors, and quantum confinement and nanostructures.

Ralph Hunter, in his 1952 Electrochemical Society (ECS) Presidential Address,⁵ noted that ECS Past President R. M. Burns, upon delivering the Perkin Medal address, predicted “a revolution in the electronics industry as a result of the developments of germanium”, and “the tremendous reduction in size and power requirements for the transistor when it replaces the vacuum tube.”⁶ Interestingly, 46 years later, Ian Ross recalled related discussions during the similar time frame at Bell Telephone Laboratories (BTL) as to the dichotomy of combining the smaller size (and increased operating frequency of the transistor) while seeking higher power at the higher frequency.⁷ Ross quoted Bob Wallace of BTL as:

“Gentlemen, you’ve got it all wrong! The advantage of the transistor is that it is inherently a small size and low power device. This means that you can pack a large number of them in a small space without excessive heat generation and achieve low propagation delays. And that’s what we need for logic applications. *The significance of the transistor is not that it can replace the tube but that it can do things that the vacuum tube could never do!*” [emphasis added].

Ross continued “and this was a revelation to us all. We realized that in chasing the vacuum tube, we had the wrong emphasis.”⁷ Rather, the opportunity was created by focusing on the transistor *in its own right*. The application of an invention is a powerful stimulus for innovation and development should not be restricted to the originally intended application as it may not be the most important. In a similar vein, Robert Lucky has recently noted “moreover there is no *a priori* way to determine what will tip a market. It’s a fundamental instance of chaos in group dynamics. And that makes it fundamentally difficult to predict future societal behaviors in the adoption of technologies.”⁸

Indeed, neither John Bardeen or Walter Brattain (Fig. 1), who co-discovered transistor action on December 16, 1947 in polycrystalline germanium^{4,9,10} nor William Shockley (Fig. 1), inventor of the minority-carrier injection concept on January 23, 1948 and the bipolar junction transistor,^{4,11-14} anticipated the ensuing impact of the transistor. Nor did the co-inventor’s of the integrated circuit (IC) in 1958, Jack Kilby (Fig. 2)^{15,16} and Bob Noyce,¹⁷ initially anticipate the ensuing microelectronics revolution. An excellent description of the differences between Kilby’s and Noyce’s approaches to the IC has been described.¹⁸ On the other hand, Patrick Haggerty of Texas Instruments clearly foretold the impact of the learning curve in de-

* Electrochemical Society Fellow.

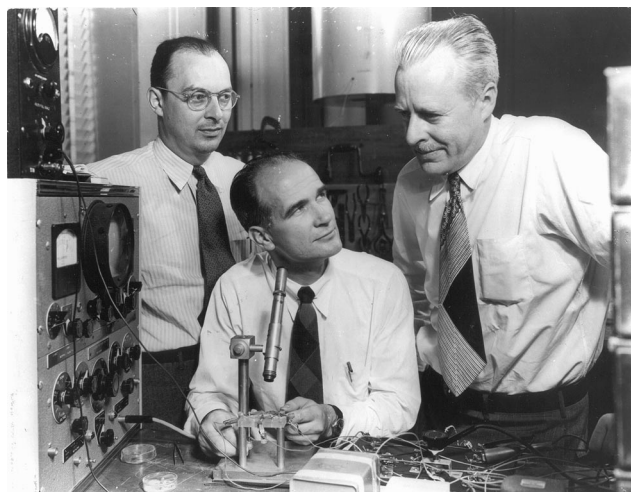


Figure 1. (From left to right) John Bardeen, William Shockley, and Walter Brattain. (Property of AT&T Archives. Reprinted with permission of AT&T.)

creasing the cost of manufacturing ICs and its increased pervasiveness in the generation of new market opportunities and the growth of the IC industry.^{15,19} Gordon Moore of Intel (Fig. 2), initially projected the growth of the number of components per chip quadrupling every two years in 1965 while at Fairchild Semiconductor Corp.,²⁰ subsequently modifying his prognosis in 1995 to about every three-to-four years.²¹ This observation, enshrined as Moore's law, became the productivity curve criterion by which the IC industry grew at approximately 25-30% compound annual growth rate (CAGR) (i.e., increased number of transistors, decreased cost per transistor.) Although Moore's law will eventually saturate, it has been the cornerstone by which the IC industry gauges its growth, as, for example, in the International Technology Roadmap for Semiconductors (ITRS).²²⁻²⁴

As a matter of historical interest, Walter Schottky comprehended the existence of a depletion region near the surface of a semiconductor in 1938, contemporaneously with Neville Mott, Boris Davidov, and shortly, thereafter, Hans Bethe.⁴ These personnel, however, focused on explaining rectification in terms of the contemporaneous space-charge theory of rectification, also referred to as the "one current" theory of rectifiers, making further scientific discussion of minority carriers at the time moot (although Davidov apparently had developed the rectification equation in 1938 ten years before Shockley^{4,25}).

J. W. Marden, chairman of the ECS Electronics Division in 1952, noted in his Editorial of The Electronics Division of the ECS that "germanium has, in like manner, found its way into the medical field and industrial applications in the production of transistors."²⁶

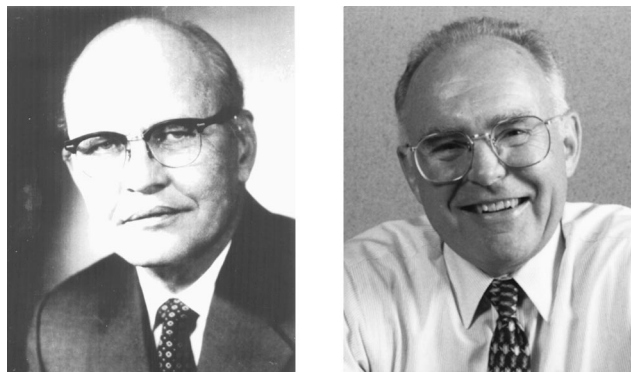


Figure 2. (left) Jack Kilby and (right) Gordon Moore.



Figure 3. (left) Robert Hall and (right) Nick Holonyak.

Additionally, Marden noted in his History of The Electronics Division that "today, the field of semiconductors has been studied very little. It is possible that by alternating currents, or otherwise, electrons may be moved from one energy level to another within atoms, in such manner that during their return to a stable condition light is emitted. Who can say that a far more efficient light source will not ultimately be produced. The function of the Electronics Division of The Electrochemical Society has been and will be to foster such new developments."²⁷

Rudolf Naby, in his assessment of the Growth of the Luminescence Section of the Electronics Division of the ECS, noted that "there is a great deal to be learned regarding the mechanisms of luminescence . . . It is predicted that many of these new discoveries will be reported before The Electronics Division and thus The Electrochemical Society will play a major role in this field."²⁸ What is truly significant was that Bardeen and Brattain's observation of transistor action on December 16, 1947, the first minority-carrier device to increase the minority-carrier concentration in a semiconductor by a current, whereas previous methods involved optical or thermal processes,⁴ facilitated both the subsequent transistor revolution and light emission from a current-driven semiconductor (although the importance of the material's band-structure was yet to be comprehended.) The development of the maser, gaseous laser, and, especially, the solid-state laser, revolutionized the communications industry. The solid-state laser was concurrently reported by four groups in 1962; Robert Hall (Fig. 3) (GaAs), Marshall Nathan (GaAs), Nick Holonyak (Fig. 3) (GaAsP), and Robert Rediker (GaAs).²⁹ In particular, the recent generation of III-V nitride-based Light Emitting Diodes (LEDs) and lasers, pioneered by Shuji Nakamura,³⁰ has facilitated the generation of white lighting as well as tunable wavelength lighting.

Scientific concepts developed during the quantum mechanical revolution in the early decades of the twentieth century (and during the first 50 years of the Society) subsequently led to successful commercial applications (and an extensive number of scientific publications in the *Journal of The Electrochemical Society*) during the second 50 years of the ECS. These early achievements included Albert Einstein's mathematical derivation in 1915 of his *A* and *B* coefficients describing spontaneous emission (relevant to laser operation in 1916-1917), Clinton Davisson and Lester Germer's description of matter waves via the diffraction pattern observed by electron scattering from nickel in 1927 (relevant to electron and hole transport in semiconductors as well as electron transport in metals), and the prediction of holes in semiconductors in 1931 by Allen H. Wilson, although it appears that Rudolf Peierls had anticipated their existence in 1928.

In that regard, Lawrence Addicks in his 1952 address on The Founders noted that "now, while The Electrochemical Society by definition merely stands between the chemists and the electrical engineers, in practice we seem to have become the homeland for the refugee scientists who find themselves in the misty no-man's land

between the older disciplines.”³¹ Indeed, Marden noted “Thus the Society opened its doors for new subjects and made its scientific publications available to those working in the pioneer fields of the electronic arts. This forward looking policy has and can be expected to result in the further growth of The Society, not only in membership, but also in scientific leadership.”²⁷ Finally, it was quite prescient of Thomas Callinan in his Editorial on The Electronics Insulation Division to note that “since the relative conductivity of each of these items [materials considered relevant to the Electric Insulation Division] is a function of the purity and processing involved in their manufacture, preparative methods are considered parts of Materials Dielectrics.”³² Even 50 years ago, the close symbiosis between the Electronics Division and the Dielectric Division (currently the Dielectric Science & Technology Division) was recognized.

The key unifying concept that evolved from Addick's and Callinan's observations has been especially epitomized by The Electronics Division during the last 50 years. This principle may be described in terms of the process-structure-property methodology as the unifying principle in describing solid-state (condensed) material characteristics. The process-structure-property approach, wherein the fabrication process determines the structure which, therefore, uniquely determines the material properties (electrical, mechanical, optical, chemical, thermal, etc.) is critical for the effective fabrication of ICs, optical components (lasers) as well as sub-three dimensional material configurations (*i.e.*, two-dimensional planar interfaces, one-dimensional linear arrays and point structures, either singularly or incorporated within higher-dimensional host matrices) to ensure the requisite performance, yield, and reliability.

Threshold Events

Background.—Transistor action was experimentally observed by Bardeen and Brattain in n-type polycrystalline germanium on December 16, 1947 (and subsequently polycrystalline silicon) as a result of the judicious placement of gold-plated probe tips in nearby single crystal grains of the polycrystalline material, *i.e.*, the point-contact semiconductor amplifier, often referred to as the point-contact transistor.^{4,9,10} The device configuration exploited the inversion layer (in their opinion) as the channel through which the majority of the emitted (minority) carriers were transported from the emitter to the collector. Indeed, it was Bardeen's surface state theory³³ which clarified the origin of the surface space charge region (SSCR) (*i.e.*, Schottky's depletion region) and its associated inversion layer. The grown junction single crystal germanium (bipolar) transistor followed in 1951 under Gordon Teal's leadership,^{3,34} based on Shockley's minority-carrier injection concept.^{4,11-14} Indeed, Shockley's injection patent was filed later than both transistor patents (*i.e.*, the point-contact semiconductor transistor patent and the bipolar junction transistor patent) and yet was awarded on April 4, 1950, earlier than the transistor patents, attesting to the importance (and recognition) of the injection concept.^{4,35}

The point-contact transistor was manufactured for 10 years starting in 1951 by the Western Electric Division of AT&T.⁷ The *a priori* tuning of the point-contact transistor parameters, however, was not simple inasmuch as the device was dependent on the detailed surface structure and, therefore, very sensitive to humidity and temperature as well as exhibiting high noise levels. Accordingly, the devices differed significantly in their characteristics and electrical instabilities leading to “burnout” were not uncommon.³⁶ With the implementation of crystalline semiconductor materials in the early 1950s,^{1,3,4} however, p-n junction transistors began replacing the point-contact transistor, silicon began replacing germanium³⁶ and the transfer of transistor technology from the lab to the fab accelerated.

Single-crystal growth.—Polycrystalline germanium and silicon were the basic materials used at BTL and elsewhere for transistor research and development inasmuch as the utilization of single crystals of germanium and silicon for the transistor was a very controversial matter at that time. Gordon Teal (Fig. 4), however, was a

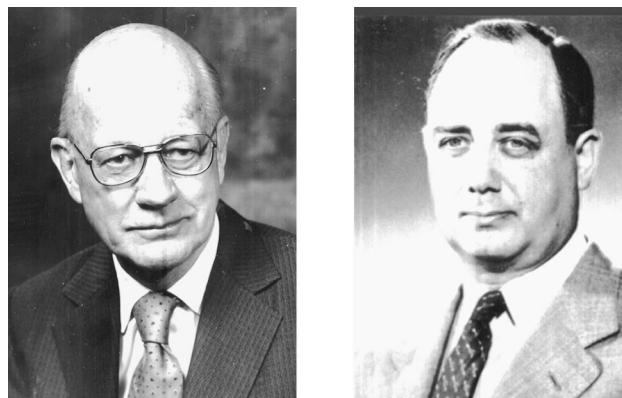


Figure 4. (left) Frederick Seitz and (right) Gordon Teal.

proponent of the criticality of single-crystal materials for the electronics era, recognizing that Shockley's bipolar junction transistor characteristics in single-crystal germanium^{37,38} and silicon³⁹ would be substantially better and more reproducible than those of polycrystalline material.^{1,3,4,40} Teal believed the fundamental property of a crystalline semiconductor which would result in its technological importance was the easily controllable and spatially variable concentration, type and mobility of free carriers, which was indeed found to be the case.^{1,3,4,40}

The successful initial results obtained in the joint research program between Teal and Little, begun in September, 1948, resulted in several germanium rods with some large single crystals³⁷ as well as grown germanium p-n junctions³⁸ by pulling from a melt, often referred to, somewhat inappropriately, as the Czochralski (CZ) technique.¹ The use of a pulling method for germanium, a single-crystal seed and the employment of new process techniques, such as precise temperature control of the melt-solid interface, were vital factors in the attainment of single-crystals in which the essential semiconducting properties became highly controlled. The preparation and characterization of single crystal material, furthermore, facilitated experimental verification of a number of quantum theoretical concepts developed for electrons and holes in crystalline semiconductors such as effective mass, drift and conductivity mobility, carrier lifetime and tunneling³ and clarification of number of phenomena in p-n junctions⁴¹ and, indeed, exhibited significantly improved characteristics compared to polycrystalline samples. The conversion of germanium and silicon ores to metallurgical grade material and their subsequent purification during the 1940s has been reviewed by Frederick Seitz (Fig. 4) and colleagues.^{42,43} By the early 1950s, all investigators of the semiconducting properties of germanium and silicon preferred to use pulled single crystals.^{1,3}

The description of dopant distribution during single-crystal growth by normal freezing was described by William Pfann (Fig. 13), ECS Solid-State Science and Technology Awardee in 1973, via the related zone-refining techniques and classic textbook, *Zone Melting*.⁴⁴⁻⁴⁶ The relationship between the effective distribution coefficient, k_e , and the equilibrium, k_0 , distribution coefficient during CZ growth was identified⁴⁷ and subsequently related to the microscopic crystal growth rate as described by Harry Gatos, ECS President in 1967-1968 and Solid-State Science and Technology Medalist in 1975, and colleagues.^{48,49} An extensive summary of the equilibrium distribution coefficients and solubilities for a variety of elements in germanium and silicon were summarized by Forrest Trumbore (Fig. 5), the first (1970) Electronics Division Awardee.⁵⁰ The path by which the role of group III and V impurities were deduced as p- and n-type dopants, respectively, in silicon was reviewed by Jack Scaff.^{1,51} The utilization of growth rate variations in germanium by Robert Hall, Solid-State Science and Technology Medalist in 1977,^{52,53} was essential to the fabrication of p-n junctions and transistors. Since it was easier at the time to make good



Figure 5. (left) Willis Adcock and (right) Forrest Trumbore.

contact to a p-type base in an n-p-n transistor rather than to an n-type base in a p-n-p transistor, the former became commercially available, subsequently followed by the p-n-p transistor using a more complicated process.⁵⁴

Transistor fabrication.—Silicon and germanium transistors were subsequently fabricated by solid-state diffusion processes in a mesa structure.^{55,56} The grown-junction silicon transistor, introduced by Teal in 1954,⁵⁷ was subsequently described by Willis Adcock (Fig. 5) in conjunction with Mort Jones and colleagues.⁵⁸ Rate-growth single crystals of silicon, containing up to five n-p-n regions (with gallium and antimony dopants), was described for silicon transistors in 1955.⁵⁹ Silicon rapidly replaced germanium for transistor fabrication³⁶ as a result of silicon's larger energy gap which facilitated higher-temperature device operation and lower-reverse current. Additionally, silicon's oxide, SiO_2 , was insoluble in water, whereas germanium's oxide was water soluble.⁶⁰ This attribute of silicon led to the fabrication of the planar silicon transistor by Jean Hoerni,^{61,62} and facilitated its utilization in the planar process as a diffusion mask for p-n junction fabrication as developed by Carl Frosch and Link Derrick,⁶³ passivation of the silicon surface and p-n junctions intersecting the surface by Mohammed (John) Atalla and colleagues,⁶⁴ and a dielectric layer for supporting metallic conductor overlayers.⁶⁰ All the elements were now available (oxidation, diffusion, photolithography, and thermocompression bonding^{7,65} for the fabrication of junction transistors and the silicon controlled rectifier (SCR) (also referred to as the four-layer switch or thyristor), in John Moll's laboratory,⁶⁶ in conjunction with Nick Holonyak, Jr., 1983 Solid State Science and Technology Awardee.⁶⁷ The SCR, developed by John Moll (Fig. 6) in conjunction with Holonyak and colleagues has a rich history.^{68,69} Jim Early concurrently improved our understanding of the static characteristics of conventional bipolar transistors by utilizing a heavily doped, thin base such that the

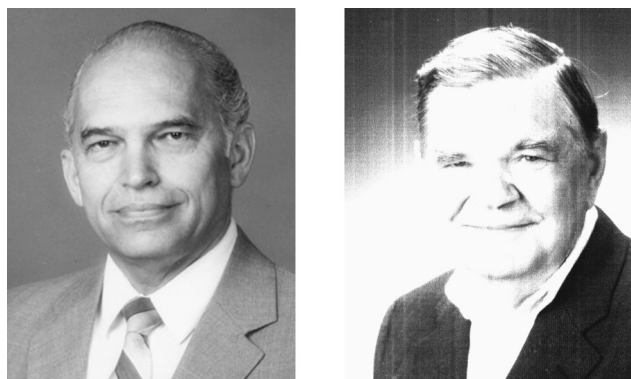


Figure 6. (left) Bruce Deal and (right) John Moll.

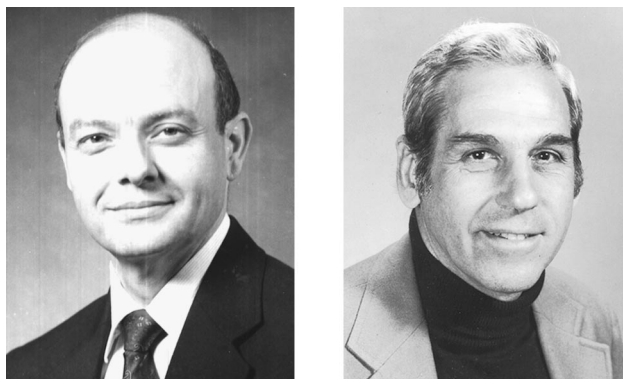


Figure 7. (left) Dennis Hess and (right) Ed Nicollian.

space-charge widening in the collector enhanced the bipolar transistor's transit time.^{70,71} The mesa and planar processes paved the way for the fabrication of the IC by Jack Kilby^{15,16,18} and Robert Noyce,^{17,18} respectively, in 1958. Henry Theurer and colleagues⁷² expanded the applicability of epitaxial structures¹ by implementing Bernard Murphy's localized, high-concentration sub-collector diffusion in the silicon substrate,^{73,74} before epitaxial deposition, which enhanced bipolar IC performance.

Precursors to the IC era.—The concurrent announcement of a practical silicon MOS (unipolar) transistor by Dawon (David) Kahng and Attala^{75,76} was based on Shockley's and earlier patents,^{1,4} quickly followed by Stefan Hofstein and Frederick Heiman's MOS IC consisting of 16 silicon n-channel MOS transistors.⁷⁷ The description of the oxidation process and methodologies for controlling the silicon/silicon dioxide interface were essential for the subsequent successful commercialization of the MOSFET and implementation of the DRAM memory era in the early 1970s. Bruce Deal (Fig. 6), ECS President in 1988-1989, ECS Fellow, recipient of the Solid-State Science and Technology Award in 1993 and the 1974 Electronics Division Award as well as the 1982 DS&T Callinan Award and Andrew Grove described the oxidation kinetics of silicon.⁷⁸ Dennis Hess (Fig. 7), ECS President in 1996-1997, ECS Fellow, and 1993 DS&T Callinan Awardee,⁷⁹ Eugene Irene, 1988 DS&T Callinan Awardee,⁸⁰ Hisham Massoud,⁸¹ co-editor of the *The Physics & Chemistry of SiO_2 and The Si- SiO_2 Interface*, and Stanley Raider, 1992 DS&T Callinan Awardee⁸² and their colleagues extended this research. Concurrently, Vik Kapoor, ECS Fellow and 1991 DS&T Callinan Awardee and William Brown, 1996 DS&T Callinan Awardee, were co-editing the ECS *Silicon Nitride and Silicon Dioxide Thin Insulating Films* proceedings, with their colleagues. Bruce Deal described the Si- SiO_2 electrical interface stability in terms of 17 types of charge mechanisms¹ and intro-



Figure 8. (left) Ken Bean and (right) Else Kooi.



Figure 9. (left) Bruce Hannay and (right) Walter Runyan.

duced the standard description for the charge notation associated with thermally oxidized silicon (SiO_2) and the Si- SiO_2 interface.⁸³⁻⁸⁵ Pieter Balk described the significance of a post SiO_2 anneal in a hydrogen bearing ambient and a nitrogen anneal in the case of the Al- SiO_2 -Si system⁸⁶ to stabilize the Si- SiO_2 interface and reduce the fixed charge, Q_f . Edward Nicollian (Fig. 7), ECS Fellow and 1986 Electronics Division Awardee, and co-author of the classic textbook *MOS (Metal Oxide Semiconductor) Physics and Technology* with John Brews, and Adolf Goetzberger described the Si- SiO_2 interface electrical properties⁸⁷⁻⁸⁸ even as others described the p-n junction under nonequilibrium conditions.¹ More recently, Yves Chabal has edited a monograph on the *Fundamental Aspects of Silicon Oxidation*, emphasizing the chemical, morphological, and electronic configuration of the Si- SiO_2 interface accompanying the silicon oxidation process, complementing the Nicollian and Brews' compendium. The LOCOS process, developed by Else Kooi (Fig. 8) and colleagues in the late 1960s,⁸⁹⁻⁹¹ was instrumental in the fabrication and achievement of superior MOS IC characteristics. Kooi summarized this enhanced IC process methodology, a mainstay for CMOS IC fabrication for more than 30 years, in the first volume of the *IEEE Case Histories of Achievement in Science and Technology*.⁹⁰

It was during this time that the Society's International Symposia on Silicon Materials Science and Technology series, the foremost Symposium describing the status, challenges, and opportunities in the advancement of silicon materials consonant with the advances in IC performance, yield and reliability, was initiated (1969), with the Ninth Symposium scheduled during the centennial anniversary of the ECS in May, 2002. Upon the occasion of the ECS's 75th anniversary, Deal and Early summarized the various device/IC configurations appropriate to that juncture.⁹² Bean (Fig. 8), Electronics Division 1988 Awardee⁹³ described his epoch research on dielectric isolation for bipolar ICs with Paul Gleim and Walter Runyan (Fig.

9).^{94,95} It was also during this time that Runyan and Grove published their classic textbooks, *Silicon Semiconductor Technology*⁹⁶ and *Physics and Technology of Semiconductor Devices*, respectively.⁹⁷ The exploding research on the physical chemistry and resulting electronic properties of single-crystal germanium and silicon (*i.e.*, crystal growth, control of composition, defects, structure, diffusion, electrical and thermal transport properties as well as surface and electrode properties) were summarized by Bruce Hannay (Fig. 9), ECS President in 1973-1974 in the classic monograph *Semiconductors*.⁹⁸ Several of the more relevant material properties of silicon and germanium were also summarized⁹⁹⁻¹⁰³ as well as a detailed review of the physics of silicon.¹⁰⁴

Finally, it should be noted that a rather innocuous observation that silicon crystals grown by the CZ method contain approximately $1.5 \times 10^{18} \text{ cm}^{-3}$ of oxygen, corresponding to 30 parts per million atomic (ppma) of oxygen¹⁰⁵⁻¹⁰⁷ (due to the etching of the quartz crucible by the molten silicon), where the oxygen concentration quoted, based on the old ASTM calibration factor, F 121-79, Annual Book of ASTM Standards, Part 43, Electronics (1979), was to have repercussions to the present day as regards wafer warpage, plastic deformation and gettering (see Oxygen in Silicon in both the Plastic Deformation and Gettering sections below).

Plastic Deformation in Silicon

Electrical effects.—Although the Teal-Little or CZ technique resulted in the growth of single crystals, there were often residual dislocations and, as it turned out, uncontrolled point defect and point-defect complexes. The detrimental influence of dislocations on planar diffused diode and transistor performance was identified by Gunther Schwuttke (Fig. 10) and colleagues to be due to excessive leakage currents (*i.e.*, soft I-V characteristics) at sub-avalanche voltages related to the precipitation of metallics onto dislocations residing in the device space charge region (SCR).¹⁰⁸⁻¹¹⁰ Schwuttke also invented the scanning X-ray oscillator technique,¹¹¹ an indispensable diagnostic procedure for studying defects in semiconductors. In a related manner, the emitter-collector leakage in narrow-base devices was shown by Fred Barson and colleagues to result from the enhanced emitter dopant diffusion along dislocations threading the emitter and collector of a transistor (pipes), which resulted in electrical shorts.¹¹²⁻¹¹⁴

The degradation of gain, increased noise of PNP transistors, and increased transistor second breakdown as well as related effects in the degradation of p-n junction characteristics due to hydrostatic pressure, uniaxial stress, anisotropic stress, mechanical damage and other structural defects have also been summarized.¹ The recovery of p-n junction characteristics due to thermal processing and the beneficial effects of gettering procedures by Goetzberger and Shockey on device¹¹⁵ and Michael Poponiak and colleagues IC characteristics¹¹⁶ were also observed.

It was eventually recognized that the device degradation associated with dislocations was dependent on the detailed nature of the method and temperature of dislocation introduction during crystal growth and/or subsequent device/IC fabrication. In the latter case, especially important factors included the temperature and temperature gradient during IC fabrication processes including the wafer cumulative history, the degree of dislocation dissociation, the structure of the dislocation core, the type and degree of impurity capture,¹¹⁷ stress effects due to the difference in size of the silicon and dopant atoms, residual peripheral latent sources of cracked dislocations, etc. John Lawrence showed that dislocations dynamically introduced during device or IC fabrication, due to the stress induced by the size difference between the silicon and dopant atom's size, were more detrimental in modifying the device microstructure and electrical characteristics than grown-in dislocations.¹¹⁸⁻¹²⁰ Freshly formed dislocations, for example, were found to enhance the emitter dopant diffusion along the dislocation, forming dislocation pipes and, thereby, resulting in emitter-collector shorts.^{112-114,120} The large number of variables noted above also contributed to the significant variability of carrier lifetime with the "same" dislocation density

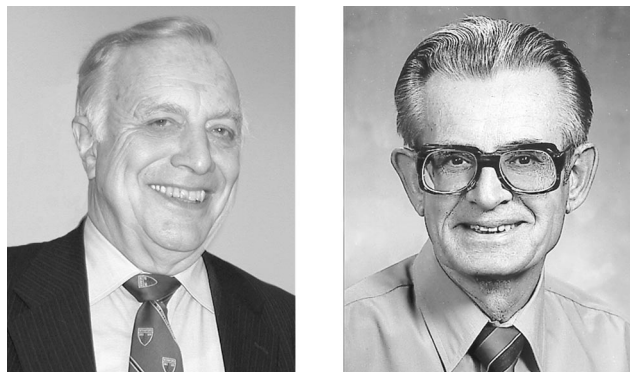


Figure 10. (left) Hans Queisser and (right) Gunther Schwuttke.



Figure 11. (left) Bob Brown and (right) Wilfred von Ammon.

and clarified why the direct effect of dislocations in silicon were often not observed.^{1,121,122} The role of dislocations in silicon was eventually recognized to be an extremely complex topic and interrelated with point defects and impurities.^{117,121}

The sum total of a large number of such observations, from the mid-1950s to the mid-1960s, was interpreted as requiring the use of dislocation-free silicon. The availability of dislocation-free material, however, did not necessarily improve the device/IC performance or yield,¹²³ which led to the “point-defect dilemma” enunciated by Erhard Sirtl, Electronics Division 1979 Awardee.¹²⁴ Indeed, there were indications that point-defect clusters were dominant and detrimental features of low-dislocation density wafers, consistent with earlier research that the structural perfection of dislocation-free silicon may be inferior for device characteristics compared to silicon with a moderate dislocation density, useful as gettering sinks for point defects as described by Hans Queisser (Fig. 10).¹²⁵⁻¹²⁸

Dislocation-Free Crystal Growth

Dash methodology.—The commercial introduction of dislocation-free silicon crystals in the mid-to-late 1960s was pioneered by William Dash¹²⁹⁻¹³¹ and immediately recognized as a major technological achievement. The design of heat-shielding components in the hot-zone of the crystal puller was subsequently shown to be of immense importance in controlling the temperature distribution at the melt-crystal interface (and point-defect incorporation in the growing crystal), as studied by Wilfred von Ammon (Fig. 11) and Eric Dornberger¹³² and Robert Brown (Fig. 11)¹³³ and their colleagues. Although macroscopic dislocation-free growth is maintained because the Peierls stress¹⁰³ to initiate dislocation movement is sufficiently high ($\sim 10^{-2}$ of the bulk modulus), temperature fluctuations can induce both microscopic point-defect fluctuations in silicon, variously described as growth spirals, growth cores, swirl



Figure 12. (left) Ken Benson and (right) K. V. Ravi.

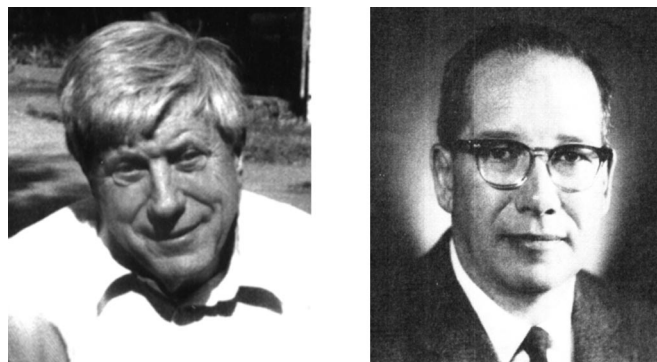


Figure 13. (left) Ron Newman and (right) William Pfann.

and striations,^{1,121} as well as fluctuations in diameter. The diameter fluctuations could be a considerable source of raw silicon yield loss, because a centerless grinding process was required to subsequently shape the grown crystal to a constant diameter. Sensing mechanisms and feedback procedures, therefore, to minimize temperature fluctuations at the melt-crystal interface received considerable attention.

Swirl is a generic term referring to a class of defect structures in silicon developed as a result of the condensation of point-defect complexes formed via solid-state reactions in the absence of readily available line and/or surface sinks and garnered extensive attention.¹³⁴⁻¹³⁹ The defects distribute in a swirl pattern, reflecting the combined effects of melt convection, rotation of the crystal and temperature fluctuations at the crystal-melt interface during crystal growth. The observed defects reflect conditions subsequent to the complete crystal growth process, resulting from the complicated set of microscopic defect reactions in silicon. These complexities in CZ crystal growth and the dynamical properties of the silicon melt were extensively studied by Wen Lin and Kenneth Benson (Fig. 12) and colleagues,^{140,141} Sam Rea,¹⁴² and a plethora of other personnel.¹ A thermal oxidation process followed by an oxide strip and a preferential etchant is generally required to observe these defects, although electrical analysis such as carrier-lifetime mapping has also proved useful. The microdefects in silicon have distinct electrical effects as shown, for example, by K. V. Ravi (Fig. 12) and Charles Varker's studies^{143,144} and, for example, could significantly impact CCD imagers^{145,146} as discussed by Lubek Jastrzebski and colleagues.

The utilization of a magnetic field of about 0.3 T (1 T = 10^4 gauss) perpendicular to the crystal growth axis was shown to stabilize the temperature at the melt-crystal interface. Cusp magnetic field configurations have also been utilized. The magnetic field also reduces the erosion of the quartz crucible as a source of oxygen as well as reduce the thermal convection currents in the metallic-like silicon melt transporting oxygen to the solidifying crystal, thereby reducing both the magnitude of the oxygen content and increasing its uniformity.¹⁴⁷

Oxygen in silicon.—Dislocation-free samples plastically deformed similarly as samples with 10^3 dislocations/cm² as shown by Witold Sylwestrowicz.¹⁴⁸ The nucleation of new dislocations during plastic deformation was deduced to overwhelm the grown-in dislocations.¹⁴⁸ Macroscopic dislocation-free silicon crystals, however, exhibited a larger spread in the ratio of the lower-to-upper yield points compared to crystals with grown-in dislocations.¹⁴⁸ The observation that dislocation-free silicon deforms plastically, furthermore, indicated that the Frank-Read mechanism was not the only possible source of dislocations. Rather, the oxygen content, its state of aggregation and the detailed thermal process conditions, was deduced to play a dominant role in plastic deformation of CZ crystals.¹⁴⁹ Jim Patel (Fig. 13)¹⁵⁰⁻¹⁵² and Ronald Newman (Fig.

13)¹⁵³⁻¹⁵⁶ and their colleagues were just two of an extensive array of personnel studying oxygen in CZ silicon, to be further discussed below.

The disappearance of the upper yield point between approximately 1100-1300°C was interpreted as a result of the formation of SiO_x precipitates due to the supersaturated oxygen content.¹⁴⁸ Above 1300°C, however, the SiO_x structures dissociate as the degree of super-saturation decreases and the oxygen returns to its atomic form, with the concurrent recovery of both the upper and lower yield points. Detailed studies of the correlation of the precipitated oxygen on both the upper and lower yield point in CZ silicon were pursued by Koji Sumino^{121,157-160} and Yojiro Kondo¹⁶¹ and their colleagues. The functional dependence of the yield point on the dislocation speed was found to be related to the charge state of the dislocation kink and, therefore, dependent on the Fermi energy (*i.e.*, the doping level).¹⁶² The comparative values of silicon's critical shear stress at different temperatures and varying oxygen precipitate concentrations have been summarized.^{1,121,163-165} The critical stress increases with both reduced wafer processing temperature and reduced oxygen precipitation. Alternatively, oxygen precipitation can reduce the critical stress for subsequent plastic deformation by the generation of internal stresses around the precipitates. The oxygen microstructure and extent of precipitated oxygen was shown to be dependent on both material and IC thermal processes as well as equipment issues, such as the insert rate of the boat into the furnace (set a given dwell temperature), wafer spacing, thermal design of the furnace, etc.^{1,121,165,166} The dislocation structure was noted to preferentially form on the concave side of a bowed wafer by Bernard Leroy, Lawrence Dyes and Howard Huff (Fig. 14) and their colleagues.^{164,167} Excessive oxygen precipitation can also preclude effective lithographic printing due to uncontrolled wafer warpage as shown by Hirofumi Shimizu and colleagues.^{168,169} The increased utilization of rapid thermal annealing (RTA) requires attentiveness to minimize global alignment errors as well as to monitor warpage so as to minimize global alignment errors in lithography. Site flatness degradation may not be as severe, and may be corrected for by site-to-site realignment. Although a number of these observations were for significantly different wafer diameters and oxygen content, the comments were generically applicable to 200 mm and may be useful guidelines for the approaching 300 mm diam era.

In view of the importance of the oxygen content for internal gettering (IG) (see Gettering section below) and considering the influence of uncontrolled oxygen content in plastically deforming and warping the wafer, the comprehension of oxygen in silicon became very critical. Detailed investigations of the mechanisms and concentration of oxygen incorporated in the grown CZ crystal were implemented.^{1,121,149,165,170-174} The oxygen microstructure and extent of precipitated oxygen was pursued by numerous investigators, covering the oxygen range as high as $2.0 \times 10^{18} \text{ cm}^{-3}$, corresponding to 40 ppma (though typically $1.5 \times 10^{18} \text{ cm}^{-3}$, corresponding to 30 ppma) to as low as $2.5 \times 10^{17} \text{ cm}^{-3}$, corresponding to 4-10 ppma.^{1,121,149,165,170-174} The importance of concurrently reducing the carbon concentration to less than $1 \times 10^{16} \text{ cm}^{-3}$, 0.2 ppma to minimize its catalytic effects on oxygen precipitation was also noted.^{175,176}

Precipitated oxygen enhanced plastic deformation in CZ wafers, compared to float-zone (FZ) silicon (utilized for power devices), where the oxygen content is typically less than 10^{16} cm^{-3} .¹⁷² Small clusters of nitrogen in FZ crystals, however, were shown to be even more effective as regards work-hardening compared to oxygen in CZ crystals.^{172,177} Nevertheless, FZ material has not replaced CZ material as the dominant material for IC fabrication, probably as a result of the extensive experience already in place with the utilization of CZ material, the wide installed base of IC processes consonant with CZ material and the larger wafer diameter available with CZ, compared to FZ, material.

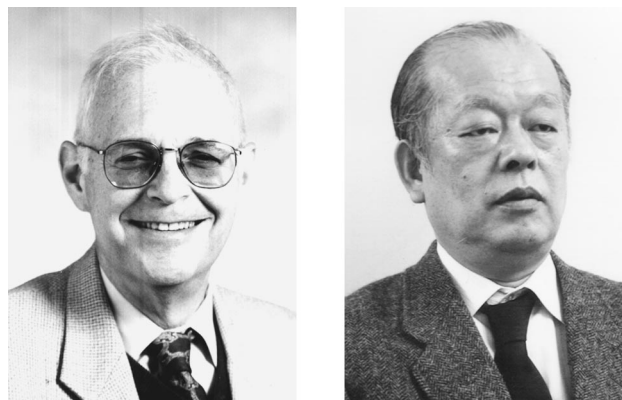


Figure 14. (left) Howard Huff and (right) Shin-ichiro Takasu.

Wafer Mechanics

The commercial introduction of dislocation-free crystals in the mid-1960s clarified the differences among dislocations; grown-in during crystal growth, introduced into the crystal during the mechanical conversion of the crystal into polished wafers, and generated in the wafer during epitaxial deposition and IC fabrication. A silicon wafer prepared for microelectronics applications requires a polished, flat upper surface free from residual edge mechanical damage and edge chips, etc. (due to the shaping processes in the conversion from the crystal to a polished wafer) and minimal residual polish damage, chemical contamination, and particulates, as well as exhibit controlled surface microroughness.^{1,121,178,179} It was experimentally found that extreme care is required to maintain the optimally prepared silicon wafer during device and IC fabrication. It was noted as early as 1966 by Schwuttke that "one should handle wafers as little as possible and use extreme care when it is necessary."¹⁰⁸ Today's 300 mm diam silicon wafers have both a polished wafer back-surface and edge. The formation of dislocations was shown to be an extremely process- and structure-sensitive parameter. Designing a wafer from a process-structure-property perspective, in order to avoid plastic deformation during IC fabrication, was usefully employed to assess, monitor and control the above variables in the multidimensional wafer and IC process space.^{1,121,165}

Radial thermal gradients developed within silicon wafers as a result of nonuniform heating during the approach to (or cooling during the descent from) the epitaxial or furnace process temperature, the insert and dwell temperatures (and strain rate due to the boat insertion/withdrawal speed) and the furnace ramp rate to the processing temperature during the furnace process. The location of wafer support points and wafer spacing in conjunction with the wafer diameter, type of boat material, and related equipment and process parameters were also critical. The furnace boat shape and the material contacting the wafers also significantly influenced the thermal gradient within the wafers. A completely enclosed boat considerably reduced the thermal gradient across the wafer by reducing the rate of heat transfer to or from the wafers.¹⁸⁰ The portion of the wafer near the contact point with the rails of the boat can exhibit a significant temperature gradient and, therefore, activate dislocation sources. This gradient is the result of both local heat flow nonuniformities due to differing thermal conductivities between silicon and the quartz glass boat¹⁶⁵ as well as differences in their coefficients of thermal expansion. The latter source acts when the silicon wafer sticks to the quartz glass boat. Plastic deformation has been noted to be more difficult to initiate at these points of contact by the utilization of silicon carbide or silicon, rather than quartz glass, boats due to the more favorable matching of the coefficients of thermal expansion.¹⁶⁵

The mathematical assessment of plastic deformation during IC fab oxidation processes was initiated by Shih-Ming (Jimmy) Hu



Figure 15. (left) Jim Amick and (right) Phil Tobin.

(Fig. 34), Electronics Division 1985 Awardee, who studied the conditions under which wafers would plastically deform, including the role of the wafer diameter, wafer thickness and wafer spacing.¹⁸¹ An extensive literature was subsequently developed,¹ including the research of Kenji Morizane and Paul Gleim¹⁸² and applications to rapid thermal processing (RTP) by Mehrdad Moslehi,¹⁸³ and Martin Schreers and colleagues.^{1,184} The pioneering studies of Runyan in 1959 showed that large diameter, 150 mm wafers could indeed be fabricated by the Teal-Little methodology,¹⁸⁵ and the procedure has morphed to 300 mm at the present time. The combined influence of thermal and gravitational stresses for 300 mm diam wafers has been extensively discussed in the 1990s and, at this time, the engineering design issues have been shown to be solvable by Huff and Randal Goodall in conjunction with Robert Nilson and Stuart Griffiths as well as by Shimizu and colleagues.^{1,160,165,186-188}

The mathematical formulation describing the thermal stress in silicon wafers during epitaxial deposition was initiated by Howard Huff and colleagues^{167,189} and extended by Jan Bloem and colleagues.¹⁹⁰ Significant improvements in epitaxial process technologies were subsequently described by Mac Robinson, Jon Rossi, Rick Wise, and their colleagues.¹⁹¹⁻¹⁹³ In light of these developments to control plastic deformation, the experimental observation by Leroy, Huff, and Dyer and their colleagues that plastic deformation could also occur in the central regions of epitaxial wafers, where no macroscopic radial gradient existed, was quite interesting.^{164,167} This was interpreted as a result of the entrapment of a hot region within a colder annular zone in a concave shaped wafer.^{164,167,194} Further examination of the front- and back-surface of the wafer indicated that dislocations moved out of the wafer and preferentially piled up on the front (*i.e.*, concave) shaped wafer surface or near the periphery area due to its larger (compressive) stress compared to the convex surface.^{164,167,194} This observation was clarified via a detailed study of the warpage of silicon wafers, induced by oxygen precipitation in wafers processed in furnaces, without the complication of a back-surface epitaxial susceptor contact.¹⁶⁴

The mechanical properties of silicon, including studies on the change in wafer shape due to process-induced warpage during wafer heating and cooling (observed to initiate at the wafer periphery and center, respectively), were summarized in the classic article by Shin-ichiro Takasu (Fig. 14), based on his research at the VLSI Technical Research Association in Japan from 1976-1979.¹⁹⁵ Minimizing the wafer warpage was shown by Shimizu and colleagues to be facilitated by reducing the insertion/withdrawal dwell temperature of the wafers to/from the furnace to less than about 850°C^{168,169} and by Phil Tobin (Fig. 15) and colleagues who illustrated the interactive effects of oxygen precipitation, wafer warpage, wafer spacing, and the push/pull temperature for critical steps.¹⁹⁶ The wafer bow was also modified not only by thermal processes or oxygen precipitation during IC fabrication but by unbalanced front and back surface film stresses resulting from the formation and selective removal of various films.¹⁹⁷ Experimental procedures were derived in the late 1960s



Figure 16. (left) Takao Abe and (right) Eicke Weber.

and early 1970s to control the activation of dislocations and subsequent wafer warpage when the boat was manually introduced into the furnace operating temperature, although the usefulness of dislocations for gettering purposes was also noted.^{1,121,165} Introduction of automatic ramp programs in the 1970s resulted in an extensive literature,^{1,121,165} indicating that 10°C/min insertion rates and 5°C/min cool rates were generally effective procedures to minimize the onset of plastic deformation for 75 mm diam wafers and a wafer spacing of 125 mils.

Point-Defect Dilemma

The introduction of dislocation-free Si wafers removed a significant source of bulk gettering sites which would have immobilized metals spuriously introduced during IC processing. The metals now preferentially segregated within the strained SCR of the device, often in conjunction with oxidation induced stacking faults, OISF,¹⁹⁸⁻²⁰⁰ and dislocation arrays introduced during IC fabrication, as described by Jim Amick (Fig. 15), ECS President in 1994-1995 and ECS Fellow.²⁰⁰ This resulted in the degradation of their electrical characteristics by modifying the electric field distribution in the p-n junction^{41,121,142} as well as degrading DRAM refresh characteristics.²⁰¹ K.V. Ravi, author of *Imperfections and Impurities in Semiconductor Silicon*,²⁰² Shyam Murarka, ECS Fellow, 1987 Callinan Awardee, and 2001 Electronics Division Awardee and colleagues^{203,204} and others have extensively described the degraded electrical characteristics of p-n junctions^{142,205-207} and gate oxide integrity (GOI),²⁰⁸⁻²¹³ due to OISFs metallic precipitates and metallic decorated structural defects such as dislocations and OISFs. Indeed, the model of p-n junction degradation due to imperfections in the SCR, metallic precipitation at LOCOS edges, trench structures and ion-implantation induced defects at spacer edges bordering SCRs, as well as on stacking faults in the p-n junction, was generally found to be more detrimental than the generation-recombination (g-r) effect of the metals, *per se*, as discussed by Bernd Kolbesen and Horst Strunk.^{1,121,214} This phenomenon, noted earlier, was described as the Point-Defect Dilemma by Erhard Sirtl.¹²⁴

Clarification began with the realization by a number of personnel that dislocations grown-in during crystal growth behaved differently than dislocations introduced during device or IC fabrication. For example, dislocations introduced during crystal growth were generally saturated with oxygen atoms, a major contaminant in silicon during CZ growth.^{117,121} Accordingly, the direct electrical effects anticipated with dislocations were often not observed, as discussed earlier.^{121,122} A moderate density of dislocations, however, did yield beneficial results in device and IC performance,^{1,121,125-128} although extensive grown-in dislocations did exhibit deleterious effects in both the fabrication and characteristics of transistors.^{1,113,121}

Over and above the point-defect dilemma, an increased understanding of the incorporation of point defects into the solidifying silicon crystal was also being obtained.^{172,215-219} The grown crystal,



Figure 17. (left) Bob Falster and (right) Vladimir Voronkov.

sectioned along the direction of crystal growth, was observed by Takao Abe (Fig. 16) to generally exhibit a spatial demarcation between vacancy-rich and interstitial-rich regions, depending on the crystal growth parameters.^{172,215-219} This demarcation region was observed as OISF generated during subsequent thermal processes by Eric Dornberger and von Ammon.²²⁰ The degradation of GOI due to OISF, generally decorated by metals, was noted earlier.²⁰⁸⁻²¹³ Vacancy-rich CZ material was also shown to result in GOI failures in 20 nm oxides, due to the agglomeration of the vacancies into macroscopic voids and related structural defects which can lead to thinning of the gate oxide as well as other intermediate structures.^{2,221} Gate oxide integrity in the sub-2 nm oxide regime, however, appears to be independent of COPs and metals,² limited instead by intrinsic phenomena such as direct tunneling. The identification of vacancy agglomerates with crystal originated pits (COPs)²²²⁻²²⁴ and flow pattern defects (FPDs),²²⁵ including their modeling with the crystal growth parameters, was also clarified.²²⁶⁻²²⁸ Post-growth annealing in a hydrogen ambient has been utilized for annihilating near-surface COPs.²²⁹

Concurrently, Kolbesen and Dolf de Kock and their colleagues²³⁰⁻²³² showed that swirl defects in FZ silicon (referred to as A defects) were interstitial, rather than vacancy, dislocation loops and by their detailed models, showed that the A and B defects were significantly different. That is, the A defects were generated by the agglomeration of silicon interstitials. The B defects were suggested to originate from dropletlike agglomerates of interstitials by Jun-ichi Chikawa and colleagues,²³³ which subsequently converted to the A defects, although the experimental conditions by which the former deduction was made does not appear to truly correspond to the conditions present during conventional crystal growth. Nevertheless, these studies on FZ material yielded a generic insight into crystal growth which became helpful for subsequent CZ studies.²³²

Tuning the crystal-growth parameters was subsequently shown by Vladimir Voronkov (Fig. 17) and later, in conjunction with Robert Falster (Fig. 17), to result in either vacancy-rich or interstitial-rich material.^{234,235} Interstitial-rich material was found to result in an improvement in GOI, although the IC DRAM yield might decrease because the IC processes utilized had been previously developed for the case of vacancy-rich material. Changing from a vacancy-rich material to an interstitial-rich material (for the same IC process flow) presumably facilitates the formation of interstitial dislocation loops which, if localized in the device SCR and decorated by metallic impurities, could lead to leakage currents degrading IC performance and yield. Re-engineering the IC process flow to be consis-

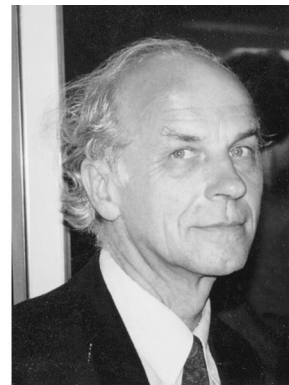
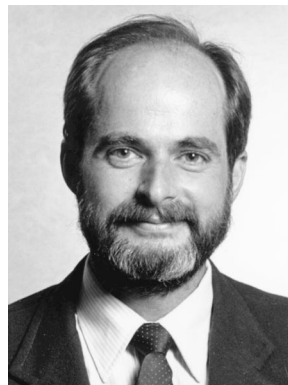


Figure 18. (left) Carlton Osburn and (right) Wolfgang Schroter.

tent with interstitial-rich material may, therefore, be required. The crystal-growth conditions resulting in either a vacancy-rich or interstitial-rich material was found to be dependent on the ratio of V/G , as a function of radius, where V is the microscopic crystal growth rate and G is the thermal gradient at the crystal-melt interface. The parameter, V/G , was shown by Voronkov and Falster to be the deciding factor as to which of the two species survives and, hence, which type of defects develop in the growing crystals. When $(V/G)(r)$ is greater than a critical number ($1.34 \times 10^{-3} \text{ cm}^2/\text{min-K}$ or $2.2 \times 10^{-3} \text{ cm}^2/\text{min-K}$), vacancy-rich material results, as described by von Ammon and Eric Dornberger¹³² or Hourai²³⁶ and their colleagues, respectively. When $(V/G)(r)$ is less than the critical number, interstitial-rich material predominates.^{132,236} Numerous discussions about the validity and relevance of the V/G parameter have been going on for more than a decade and Voronkov's approach is widely accepted. As most of the thermophysical properties cannot be directly measured, however, an extensive effort has been carried out to theoretically calculate V/G , including the detailed mechanism wherein the interstitial or vacancy are dominate as well as the formation of the OSF ring by Abe Brown, Talid Sinno, Ryuichi Habu, and their colleagues.^{217,237,238} Nevertheless, Abe and co-workers have noted the greater importance of the thermal gradient, per se, at the crystal-melt interface in controlling the formation of point defects.^{215-218,239} In any case, the controlled use of after-heater heat shields and the growth of a crystal such that small numbers of both vacancies and interstitials are formed (i.e., no point-defect clusters) is preferred.

Gettering

Background.—The diffusion, solubility and electrical activity of transition metals in silicon have been extensively studied by Eicke

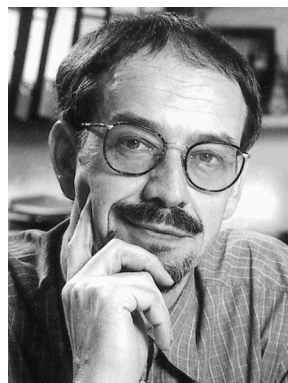


Figure 19. (left) Ulrich Gosele and (right) Werner Kern.



Figure 20. (left) Alain Diebold and (right) Linus Kimerling.

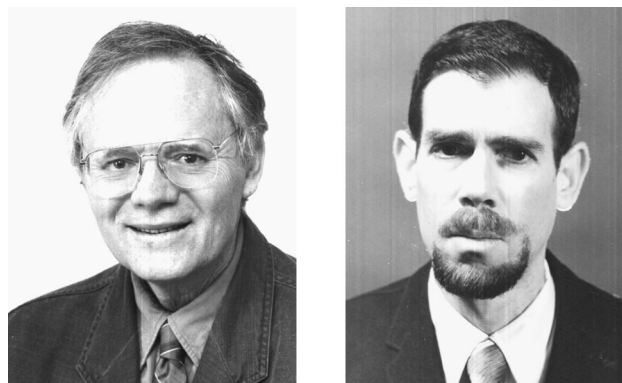


Figure 21. (left) George Rozgonyi and (right) Ted Kamins.

Weber (Fig. 16) and Wolfgang Schroter (Fig. 18) in conjunction with their colleagues as well as other personnel^{1,240-242} and summarized by Klaus Graff.²⁴³ Weber has shown that the transition metals exhibit a significant component of interstitial, as well as substitutional, solubility. This results in a mixed diffusion process, with a fast interstitial component (interstitialcy mechanism). The 3d transition metals in silicon, such as iron and chromium, mainly occupy and diffuse via interstitial sites. They accordingly exhibit high diffusion coefficients. Cobalt, Ni and Cu diffuse sufficiently fast, even at 27°C, that these elements could transfer from interstitial sites onto dislocation sites as well as form clusters and precipitates. Copper, however, appears to be especially different from the other 3d metals and has recently been extensively reviewed by Andrie Istratev and Weber, illustrating the insights and changes in our interpretation of experimental Cu diffusion data in silicon over the last 40 years.²⁴⁴ The 4d metals in silicon, such as Ag, exhibit a solubility on substitutional sites comparable to interstitial sites and, therefore, diffuse slower than the 3d transition metals. The 5d metals, such as Au and Pt, exhibit a dominant substitutional solubility. The 5d metals accordingly take a longer time until their substitutional solubility is attained throughout the wafer. Size effects and electronegativity differences between the impurity and host atoms are also important considerations and must be taken into account for these analyses.

The U-shaped diffusion profile of Au is clear evidence that there is also a fast diffusing interstitial component for the 5d metals. The lack of sufficient interstitial sinks in dislocation-free silicon limits the kinetics of the transfer of Au onto substitutional sites during diffusion. The diffusion mechanism in the case where the impurity occupies both substitutional and interstitial sites was expanded from the conventional mechanism wherein an interstitial metal combines with a vacancy to occupy a substitutional site. The new phenomenon, identified by Ulrich Gosele (Fig. 19), Electronics Division 1999 Awardee, involved an interstitial metal transferring to a substitutional site ejecting an interstitial and was referred to as the kick-out mechanism, (alternatively a substitutional metal combining with an interstitial wherein the metal transferred to the interstitial site).²⁴⁵⁻²⁴⁷ Masaki Aoki showed that the temperature dependent solubility and diffusion coefficients, taking into account kinetic considerations during cool-down from high-temperatures, are especially important for transition metals such as Fe in determining their state of aggregation at room temperature.²⁴⁸

Metallic impurities can affect the electrical resistivity of silicon if they are present in sufficiently large enough concentrations (much greater than 10^{15} cm^{-3}). Metal concentrations in the range of 10^{15} cm^{-3} are generally more important as traps or g-r centers which can degrade a number of device characteristics. Today's high-quality materials, however, typically have much less than $10^{12} \text{ metals/cm}^3$, corresponding to significantly less than $10^{10} \text{ metals/cm}^2$. Process-induced contamination is often the most catastrophic effects of metals due to their localized coagulation or precipitation on defects in p-n junctions or near the channel region

of an MOS device. Metallic contamination by Fe, Ni, and Cu in the range of 10^{11} - 10^{13} cm^{-2} during ion implantation, dry etching, and plasma CVD, however, is much more likely to be introduced onto the wafer surface during wafer preparation or IC fabrication. In fact, Paul Schmidt and colleagues showed that metallic impurities can also be introduced from the furnace per se, let alone from handling tools, carriers or other tools utilized in the fab.^{249,250} The surface metals diffuse into the wafer bulk during subsequent thermal processing. The surface and bulk descriptions, however, cannot be simply transposed via the wafer thickness due to surface-bulk segregation during thermal processing. In view of this, prescriptions are under development to determine the equivalent bulk concentration from a given surface concentration during subsequent thermal processing. The comprehension of the redistribution of metals between the surface and bulk during IC thermal processing, dependent on surface cleaning methodologies (and sequence) is receiving increased attention and is especially important as regards lifetime doping. An extensive methodology has developed for the removal of surface metals by cleaning with suitable solutions of high-purity chemicals, as initiated by Werner Kern (Fig. 19), ECS Fellow and DS&T Callinan Awardee in 1972, editor of the influential *Handbook of Semiconductor Wafer Cleaning Technology* and colleagues.²⁵¹

A set of defect/diagnostic tools for IC process evaluation has been reviewed by George Rozgonyi.²⁵² The sensitivity of surface diagnostic techniques varies, but was shown by Alain Diebold (Fig. 20) co-editor of the NIST series on *Characterization and Metrology for ULSI Technology*, and colleagues to range between 10^8 - $10^{10} \text{ atoms/cm}^2$ for a variety of transition metals.²⁵³ A useful qualitative diagnostic technique to detect the presence of metals was accomplished by monitoring the etch pit density with a large concentration of metals present, conventionally referred to as "haze" as measured by the modulated optical reflectance technique.²⁵⁴ More quantitative results were available by monitoring the carrier lifetime and electron beam induced current (EBIC). The utilization of EBIC techniques have been useful to assess the electrical activity of the various microstructures fabricated to getter the undesired impurities from the device active regions. Junction capacitance and current spectroscopy procedures were pioneered by Chin-Tang Sah and colleagues.²⁵⁵ Deep level transient spectroscopy (DLTS) has become a major diagnostic tool to identify the energy levels of the various chemical impurity-structural defects in the majority-carrier half of the band-gap. L. C. Kimerling (Fig. 20), Electronics Division 1995 Awardee, in conjunction with Janet Benton and colleagues have developed an extensive catalog of the energy levels for these structural-chemical complexes in the band-gap of silicon, based on the DLTS methodology.^{256,257}

Gettering provides a mechanism to remove these process-induced metal contaminants from active device regions and has been correlated with significantly improved device performance, yield and reliability.^{1,121} These benefits were observed in p-n junction device characteristics,²⁵⁸⁻²⁶⁰ oxide leakage current and breakdown,²⁶¹

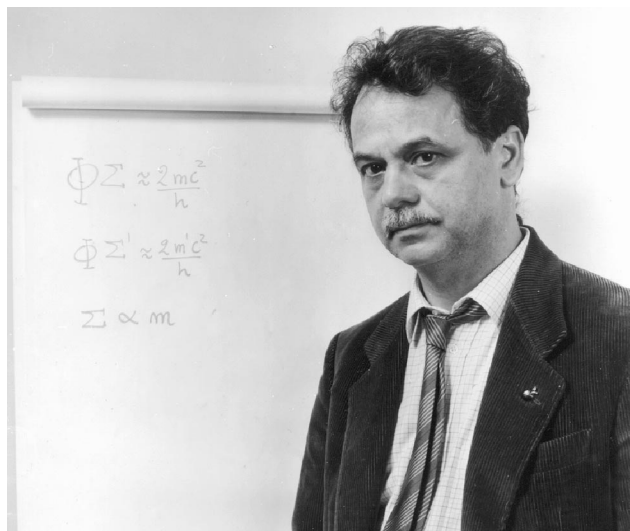


Figure 22. Geofranco Cerofolini.

MOS dynamic shift register leakage currents,²⁶² DRAM refresh time,^{201,263} CCD imager performance by collecting minority-carriers generated by spurious radiation,¹⁷⁵ and CMOS circuit latch-up control by reducing the recombination lifetime in the substrate.²⁶⁴ Significant improvements were observed in MOS,²⁶³ bipolar,²⁶⁵ and CPU ICs.²⁶⁶ Louis Parrillo and colleagues described the integrated benefits of detailed attention to optimizing the response of the silicon wafer to the full suite of bipolar fabrication processes beyond just gettering, in order to achieve optimal IC performance.²⁶⁵ The development of quantitative gettering processes and models were especially helpful in gaining insight into the microphysical processes operative, although continuous refinements ensure this will remain an active area of research.^{260,267-272} Thomas Seidel, in particular, clearly enunciated at the 156th, Fall, 1979 meeting of The Electrochemical Society's Gettering symposium, that successful gettering required three essential steps. These steps were the release of metals from their deleterious location within/near the device, transport of the metals to the gettering arena (sufficiently removed from the spatial location or SCRs of the device), and capture at the gettering site (and retention during subsequent thermal processing.)

Gettering methodologies (nonoxygen techniques).—The concept of gettering to improve device performance was actually implemented before the point-defect dilemma had been appreciated. The first reported instance of gettering in silicon appears to have been the utilization of a phosphosilicate glass (PSG) film on the back surface of the silicon wafer by Goetzberger and Shockley to getter unwanted metallic impurities away from the device active regions.¹¹⁵ It was initially believed that the metallic impurities were incorporated within the PSG liquidus. PSG gettering was also utilized in n-channel DRAMs as a result of the introduction of P via POCl_3 doping of the n-type source/drain. It subsequently became clear that gettering was due to metallic incorporation within the misfit dislocation array, formed as a result of the size difference between the tetrahedrally covalently bonded silicon (0.118 nm) and phosphorus (0.11 nm) atoms, when the diffused sheet resistance was less than about 4 ohms/sq.

A variety of back-surface external gettering (EG) mechanisms were subsequently examined,¹ especially mechanical damage,¹³⁷ ion-implant damage,^{273,274} polysilicon gettering²⁷⁵ and, to a much lesser extent, nitride gettering²⁷⁶ and laser damage gettering.²⁷⁷ The pre-eminent technique, however, was a variety of methodologies collectively referred to as preoxidation gettering procedures (POGO), as exemplified by George Rozgonyi (Fig. 21), ECS Fellow and Electronics Division 1981 Awardee and colleagues.²⁷⁸ External



Figure 23. (left) Cor Claeys and (right) Arnold Reisman.

gettering was found to be useful, although some procedures were often limited temporally due to the decrease in gettering efficiency with continued thermal processing. With the reduction of IC fabrication temperatures to below 1000°C, for example, PSG gettering becomes less effective and various combinations of the above methodologies were extensively examined.^{1,279} The mechanical damage procedure, however, was prone to particulates flaking off the back-surface. Back-surface polysilicon gettering was a cleaner procedure and was extensively utilized. Theodore Kamins (Fig. 21), ECS Fellow and Electronics Division 1989 Awardee has discussed the properties and utilization of polysilicon, especially for the gate electrode for CMOS devices and the interpoly electrode for EEPROM devices.^{280,281}

Interestingly, POCl_3 diffused samples at 1100°C and annealed at 800°C was noted by Geofranco Cerofolini (Fig. 22), co-author with Laura Meda of the textbook *Physical Chemistry of, in and on Silicon*, and colleagues to contain a complex network of dislocations and defects which were deduced to be effective gettering sites for reducing the leakage current in diodes.²⁸² Subsequent research reduced the POCl_3 deposition temperature to 920°C, followed by the 800°C anneal which resulted in a significant increase of the MOS capacitor storage time, of significance for DRAMs.²⁸³ Concurrently and independently, Huff and co-workers used POCl_3 deposition at 1100°C or 1000°C, followed by a low-temperature N_2 anneal in the range of 700°C, for the fabrication of 16K DRAMs and also observed significantly improved MOS capacitor storage times.²⁸⁴ The TEM micrographs of James Mayer and colleagues were a very useful visual representation of the bulk microgettering network,²⁸⁵ consistent with the hypothesis current at the time.

Back-surface ion-implantation gettering was also successfully introduced, although as noted above, the healing of the ion-implant damage during subsequent thermal processing required multiple implants during IC fabrication. It was observed by Henry Geipel and Warren Tice that since the dislocation energy is proportional to the square of the Burger's vector, perfect dislocations were more effective than partial dislocations for gettering;²⁸⁶ moreover, the heavier the ion, the more effective the gettering. Accordingly, argon damaged layers were particularly favored for this technique and found to be more effective for gettering Au than POCl_3 gettering at temperatures below 1000°C, whereas the two mechanisms were about equal from 1000°C to about 1150°C.²⁷⁹ Experimental data by Yasuteru Ichida and colleagues indicated that a POCl_3 gettering process introduced at the end of device fabrication was more successful than its introduction at the initiation of the device fabrication process.²⁸⁷

HCl gettering, introduced by Rudolf Kreigler, DS&T Callinan 1979 Awardee, became an especially prevalent industrial technique.²⁸⁸⁻²⁹⁰ Carlton Osburn (Fig. 18), ECS President in 2000-2001, ECS Fellow and recipient of the Electronics Division Award in 1991 and the DS&T Callinan Award in 1975, has studied the improvement of GOI via Cl methodologies²⁹¹ as part of an extensive

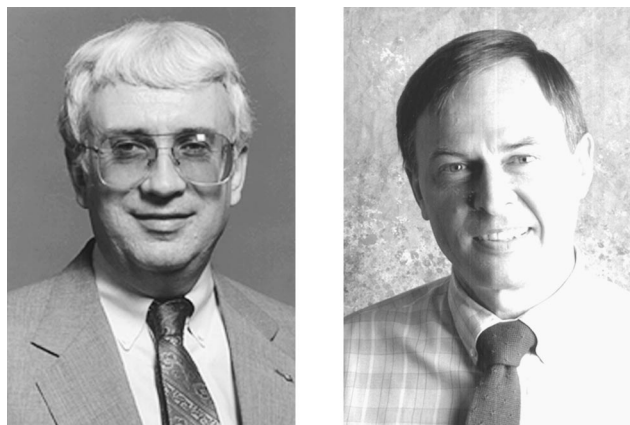


Figure 24. (left) Richard Fair and (right) Jim Plummer.

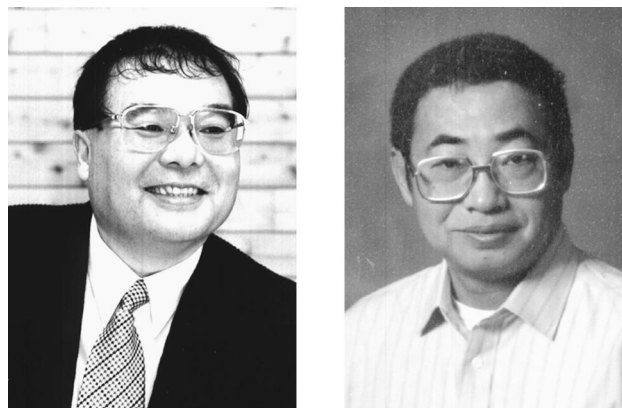


Figure 25. (left) Fumio Shimura and (right) Teh Tan.

series of analyses in the VLSI Laboratory of Arnold Reisman (Fig. 23), 2001 Solid-State Science and Technology Awardee, ECS Fellow and Electronics Division 1984 Awardee.²⁹² Gettering was initially believed to occur by formation of volatile metal chlorides, although the Gibbs free energy of formation of most metal chlorides was not negative. The Cl, however, was also interpreted as removing interstitials, as evidenced by the shrinkage of OISF at sufficiently high temperature by Hiromitsu Shiraki, Cor Claeys (Fig. 23), co-editor of the *ECS High Purity Silicon, ULSI Process Integration*, and *Crystalline Defects and Contamination* proceedings and their colleagues,^{293,294} thereby removing potential sites of metallic precipitation adjacent to the device. Jimmy Hu showed that the shrinkage (retrograde growth) of OISF at sufficiently high temperatures in the absence of HCl was dependent on both the surface orientation and ambient.²⁹⁵ It was also suggested by Kreigler that Cl was most useful for cleaning the furnace quartz tube rather than actively incorporated into the oxide due to reliability concerns.^{289,290}

A large solubility enhancement (about 10^3 times the intrinsic solubility) was observed by Meek and Seidel in heavily doped n-type silicon due to substitutional metal-substitutional donor pairing.²⁹⁶ The pairing of interstitial metal donors with substitutional acceptors in heavily doped p-type silicon, however, resulted in an increased metal solubility only one to two orders of magnitude compared to the intrinsic solubility because of increased configurational and vibrational entropy effects associated with the interstitial metal-acceptor pair.²⁹⁶ The description of this enhancement in solubility has also been described in terms of a Fermi energy effect by Aoki, Scott McHugo, and their colleagues.^{297,298} Heavily doped isolation regions also gettered metals, due to both the diffusion induced damage as well as by the solubility enhancement of metals in heavily doped regions.

The beneficial effects of implantation gettering on both the generation and recombination lifetimes, over a limited annealing temperature range, was also observed. The efficacy of back-surface abrasion damage was often found to decrease with continued thermal processing, but the technique was useful in removing swirl defects and the monitoring of various gettering mechanisms led to an extensive literature. In particular, P introduced by POCl_3 , and argon ion-implantation as well as oxygen precipitation were suggested to act as sources of silicon interstitials which mediated the transport of metals and facilitated gettering, as discussed by Jim Plummer (Fig. 24), ECS 1991 Solid State Science and Technology Medalist and colleagues in their extensive point-defect studies.²⁹⁹ In that regard, Hu's research in the 1960s and 1970s was instrumental in establishing the dual mechanism of both vacancy- and interstitialcy-mediated diffusion of group III and V elements in silicon (although there is a dominant point-defect species, dependent on the size of the diffusing element)³⁰⁰ and the interactions in sequential diffusion processes.³⁰¹

These point-defect studies of Hu have been summarized in the 1990s.^{302,303} Gettering mechanisms which inject interstitials facilitated the transfer of 5d metals which predominately diffuse by an interstitial mechanism, from low mobility, high solubility substitutional (and electrically active) sites to high mobility, low solubility interstitial sites via the transport of metals to IG or EG captive sites away from the device active regions. The role of silicon interstitials in the generation of dislocation loop gettering complexes in (low oxygen content) magnetic CZ (MCZ) and FZ silicon was also noted as well as the role of interstitials in Si by Kimerling in the promotion of a host of solid-state defect and gettering reactions.^{257,304} The chemical state of the transition metals was also noted by Kimerling to possibly be playing a role influencing their participation in various gettering schemes.³⁰⁵ The role of vacancies, however, also continues to be acknowledged as playing some role in the overall diffusion and gettering schemes. The modeling of the emitter dip effect and the emitter retardation in relation to the vacancy charge states has been discussed by Richard Fair (Fig. 24) and his colleagues's ion-implantation and diffusion studies.^{306,307} Scott Dunham has also explored the role of vacancies in transient enhanced diffusion³⁰⁸ as have others.¹

A number of other gettering techniques have been described although they have not yet been implemented into IC fabrication. These include porous gettering, cavity gettering, ultrasound gettering, electric field induced dissociation of Fe-B pairs to enhance gettering of Fe, gettering by enhanced wafer bending, and external gettering by an Al-SiO₂ film deposited on the back-surface and processed above the Al melting temperature.¹ There is also continued interest in replacing the highly doped substrate of an epitaxial wafer with an implanted ground plane (in a polished wafer) formed by an unmasked, high dose, MeV implant, which also has the potential for gettering.^{309,310} Finally, it should be noted that gettering was not quite the panacea for every application.¹

Gettering methodologies (internal oxygen gettering).—The predominant method of gettering became oxygen internal gettering (IG) with the implementation of a defect-free denuded zone (DZ) near the surface and precipitation dislocation complexes (PDC) in the bulk, as promulgated by Teh Tan (Fig. 25) and colleagues.²⁵⁸ Both high performance and yield (minimal refresh loss) was achieved in MOS DRAMs by Huff and colleagues²⁶³ by fabricating the DRAM in a sufficiently deep DZ with high generation lifetime material^{1,121} in conjunction with a small bulk recombination lifetime. The DZ should be sufficiently small, however, to ensure effective gettering by the bulk gettering sites. In addition to the improved device characteristics described in the Gettering Section, the beneficial effect of IG was also reported to control epitaxial stacking faults,^{311,312} reduce saucer pit formation,^{313,314} retard slip formation³¹⁵ and improve MOS carrier generation lifetime.^{263,316,317} Initial observations

also indicated both higher DRAM performance and yield from the lower sections of the CZ crystal.³¹⁸ A comprehensive discussion of oxygen in silicon was presented in *Oxygen in Silicon*,¹⁴⁹ edited by Fumio Shimura (Fig. 25) and in the host of studies collectively authored with his colleague Hideki Tsuya (Fig. 34).³¹⁹⁻³²²

Successful IG required understanding the mechanism of oxygen incorporation and controlling its magnitude and spatial homogeneity during CZ crystal growth. Indeed, OISF often replicated the micro-defect patterns in the grown crystal as shown by Abe and de Kock.^{172,232} PDCs formed during IG can exhibit either a positive or a negative influence on IC electronic characteristics. An excessive number of PDCs, in conjunction with too shallow a DZ, significantly degrades the IC performance. If the PDCs are located sufficiently far away from the surface (typically $>30\text{ }\mu\text{m}$ below the active device area), they can provide sites, due to the localized crystal disruption, for gettering metallic impurities inadvertently introduced during IC fabrication. Accordingly, process engineers aggressively pursued identification of the optimal oxygen concentration (and degree of super-saturation),^{1,121,172} the role of dopant type and concentration as regards the influence of the point-defect density in promoting SiO_x precipitation,³²² the associated IC thermal processes (temperature, ambient and sequence), the usefulness and mechanisms of high-temperature annealing and out-diffusion (including the role of hydrogen, argon or nitrogen annealing),²²⁹ and nucleation and growth procedures (including the role of ramp-up (and to a lesser extent cool down) techniques to process temperature) to make the gettering process more robust, as described by Seigo Kishino and colleagues.^{1,267} In particular, nucleation and growth processes were mainly heterogeneous processes, including carbon¹⁷⁵ (and perhaps other impurities) as participants in providing thermodynamic pathways in addition to that provided by interstitials.^{149,323} In that regard, the slower oxygen precipitation rate in n/n^+ material (occasionally attributed to the difficulty of incorporating oxygen in highly doped antimony crystals), (although doping species and related electrical effects have also been proposed) is especially enhanced by ramping procedures.

Quantitative modeling of the IG gettering efficiency with the density, morphology, and distribution of bulk microdefect structures (including their dependence with the concentration of oxygen and the role of the nuclei size distribution for condensed matter aggregation phenomena) was extensively studied by Fujimori.³²⁴ It was also noted by William Patrick and colleagues that whereas devices processed from wafers near the seed end of a crystal eventually lost its gettering efficiency, devices from wafers from the tail end of the crystal (with a lower initial oxygen content) initially exhibited higher leakage currents, but with extended thermal processing, generated sufficient SiO_x precipitates to eventually exhibit lower leakage currents than wafers from the seed end of the crystal.³²⁵ Internal gettering, however, does not perform as an infinite sink inasmuch as gettering will stop when the metal concentration in the DZ approaches the thermal equilibrium solubility,²⁴⁸ consistent with the process kinetics, although this potential limitation continues to be explored.

The relationship of the various thermal processes associated with IC fabrication, in conjunction with the thermal donor anneal, historically performed at $\sim 625^\circ\text{C}$ for 30 min or so by the silicon wafer supplier (as well as, recently, via an RTA), led to an escalating number of publications postulating a host of solid-state reactions. A particular popular IC thermal process sequence became known as the hi-lo-mod hi process, in view of its compatibility with IG gettering. The initial hi temperature process facilitated the out-diffusion of oxygen and was characterized in terms of $(\sqrt{Dt})$, where D is the diffusion coefficient of oxygen and t is the time of the process). The low-temperature step, about $600\text{--}700^\circ\text{C}$, nucleated the bulk IG centers while the subsequent high-temperature anneal facilitated the growth of these bulk nuclei. At this point, the DZ could be readily distinguished by an appropriate etching or electrical technique, although the growth of these bulk nuclei continued to some extent

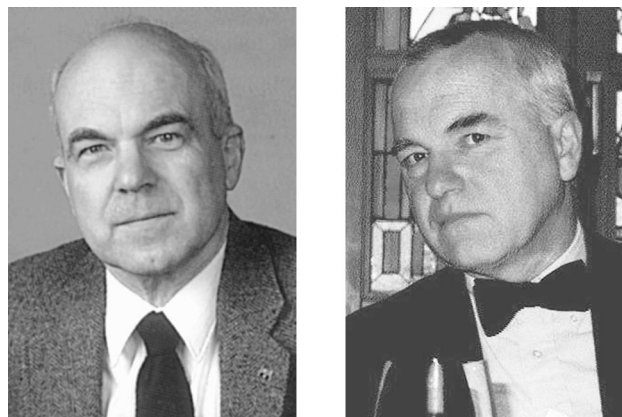


Figure 26. (left) W. Murray Bullis and (right) Laszlo Fabry.

with further IC thermal processing. The second high-temperature anneal was generally less than the initial high-temperature anneal so as not to dissolve those nuclei which were thermodynamically stable at the higher temperature. Of course, one may imagine many scenarios for the stabilization of the bulk gettering nuclei and IG gettering. John Borland has described an extensive number of macroscopic processes to enhance the IG methodology³²⁶ while Edward Wijaranakula and John Matlock have described a number of the microscopic processes associated with the IG methodology.³²⁷

The role of the ambient during the IG out-diffusion procedure was shown by Hu to be an especially important parameter.³²⁸ For example, argon and nitrogen ambients facilitate the out-diffusion of oxygen from the bulk of the wafer; if the oxygen content of those ambients is sufficiently low (*i.e.*, low fugacity). In this case, the surface oxygen content is pinned to a value less than that obtained during an oxygen anneal. This methodology has also been helpful in improving the surface quality, reducing OISF and improving GOI. A hydrogen ambient has been noted to be useful in promoting the out-diffusion of oxygen as well as facilitating the surface phase reaction responsible for both perpendicular configurations of fingers often observed on epitaxial silicon surfaces along with improved surface quality.¹

Epitaxial Material

Epitaxial material such as p/p^+ suppresses latch-up, and improves GOI and DRAM refresh performance compared to polished wafers^{1,121,172,329-331} and, accordingly, has often been the material of choice for logic ICs such as ASICs, microprocessors, and EEPROMs. The onset of trench isolation, however, has reduced somewhat the concern over latch-up. The increased cost of epitaxial materials has been more than offset by the performance (and price) of these leading edge ICs. Although DRAMs were initially fabricated in polished wafers, epitaxial material became the material of choice for DRAMs during the first half of the 1980s, at least for U.S. manufacturers. The perceived benefits were the readily available latch-up control (U.S. manufacturers utilized the same design rules for both the n-MOS memory and the CMOS periphery circuitry) and the improved benefits of a heavily doped substrate in reducing the diffusion current (see Carrier Lifetime section). Japanese DRAM manufacturers, however, opted for polished wafers, due to the lesser performance requirements of DRAMs compared to logic ICs, and the attendant commodity pricing strategies. In this case, latch-up control was probably achieved by larger design rules for the periphery CMOS circuitry as well as, perhaps, by utilizing selectively diffused or implanted guard rings. U.S. DRAM manufacturers subsequently returned to polished wafers in the mid 1980s due to the severe DRAM pricing strategies. The beneficial reduction in the price ratio of epitaxial material compared to polished wafers, may be anticipated to continue its decline for 300 mm wafers, although

the utilization (and cost) of MCZ substrate wafers may be increasing faster than the decreasing cost of the epitaxial wafer deposition process, per se.

The improved GOI in epitaxial material, initially considered to result from its reduced surface microroughness specified over a defined spatial frequency range,^{178,179} is now believed to result from, at least partially, the improved structural perfection of the epitaxial material, as compared to residual polishing damage in polished wafers. The utilization of p/p⁻ epitaxial material for DRAMs is also receiving attention; the benefit of improved surface quality and reduced system capacitance may offset the lack of Fermi-energy enhanced solubility gettering of Fe observed in the p⁺ substrate of the conventional p/p⁺ epitaxial system.^{297,298} If significant IC benefits are perceived and implemented, the IC industry will successfully cope with the absence of solubility enhanced gettering. The oxygen content, however, may have to be re-assessed in the case of the p/p⁻ system since the influence of IG has been considered to be superior in p⁺, compared to p⁻, material.^{332,333} Clarification of the enhanced oxygen precipitation in p⁺, as compared to p⁻, substrates has been related to a larger total quantity of precipitated structures in the former case,³³² whereas the strain around the precipitated complexes has been shown to be less in p⁺, compared to p⁻, material.³³²

The role of MeV implantation and associated annealing procedures in polished wafers as a replacement for epitaxial structures continues to receive attention, although the control of COPS and related defects will be aggravated in polished wafers. Indeed, the use of MeV implant/anneal procedures, in some cases in conjunction with epitaxial wafers, has been proposed to achieve enhanced device architectures,^{309,310} although the implementation of this procedure has been somewhat slow to date.

Carrier Lifetime

Gold has been an especially critical element for controlling the carrier lifetime in silicon, as summarized by W. Murray Bullis (Fig. 26), ECS Treasurer, 1994-1997 and co-editor of the ECS *Defects in Silicon* proceedings.³³⁴ Structural irregularities like OISF were also identified as significantly degrading carrier-lifetime.³³⁵ Although this reference relates to GaAs, the result is generically applicable to Si, albeit with greater sensitivity to the degree of metallic decoration of the partial dislocations associated with the stacking fault, see Ref. 122. Alvin Goodman implemented a series of studies on the constant magnitude steady-state surface photovoltage (SPV) method for silicon,³³⁶ determining the bulk recombination lifetime via the measurement of the minority carrier diffusion length and utilization of the Einstein relation. A variant of this method in which the surface photovoltage varies and the impinging photon flux is fixed has also been described.³³⁷ The pulsed MOS capacitor generation lifetime technique, introduced by Manfred Zerst,³³⁸ is widely used because the MOS capacitor is utilized on most test structures. The relation between the recombination and generation lifetimes and related diagnostic techniques has been extensively studied by Dieter Schroder.^{337,339,340} In a somewhat complementary fashion, Bullis and Huff have assembled the more common carrier lifetime techniques, their benefits and limitations on their interpretation as well as a proposed unified taxonomy.³⁴¹ Finally, the extensive studies of Claeys and colleagues of the influence of the perimeter to area ratio in determining the various lifetimes in scaled devices is of particular significance.³⁴²

Appropriate gettering procedures were implemented to both retain and improve the carrier lifetime. The carrier recombination lifetime is a particularly sensitive technique to assess the DZ quality. The recombination lifetime has also been extensively utilized to assess the interstitial Fe_i content by monitoring the Fe_i-B neutral pair species versus the significantly more electrically active Fe_i content by Gunther Zoth and Werner Bergholz³⁴³ and extensively implemented by Jastrezbski and colleagues.³⁴⁴ Both thermal and, more recently, optical techniques have been utilized to destroy the Fe_i-B pair.^{343,344}

The carrier-lifetime for DRAMs requires consideration of two apparently contradictory requirements.³³⁰ In one case, a high (generation) lifetime is desired to facilitate the retention of charge for an extended period of time (i.e., high DRAM circuit refresh time). On the other hand, high (generation) lifetime material is especially susceptible to discharge of the DRAM storage node and, thereby, loss of information content due to transient electronic phenomena. A compromise is required for optimal DRAM performance. Internal gettering, in conjunction with the formation of the DZ, can reduce the influence of the transient phenomena while increasing DRAM performance and yield. This is accomplished by fabricating the DRAM and its voltage-dependent SCR in an appropriately deep DZ of sufficiently high (generation) lifetime material while, concurrently, maintaining the DZ sufficiently shallow to ensure effective gettering by the bulk gettering sites (and collection of carriers due to the low recombination lifetime). The lifetime in the DZ, called the generation lifetime, τ_g , and sampled within the voltage-dependent SCR of the IC, can be rather high due to the IG/EG in the silicon wafer. Concurrently, the recombination lifetime, τ_r , in the bulk of the wafer, sampled over the minority-carrier diffusion length, can be readily modified (decreased) via the nature of the gettering procedure utilized.

Because ICs typically operate in the temperature range of 75°C, the contribution of the diffusion current from the bulk becomes an important factor due to the exponential increase in n_i^2 with increasing temperature. A significantly reduced bulk recombination lifetime, τ_r , due to IG, for example, would increase the diffusion current; increased substrate doping, such as in a p⁺ substrate, however, substantially decreases the diffusion current as discussed by Pallab Chatterjee and colleagues³²⁹ as well as Hideki Iwai and colleagues.^{330,331} The utilization of a lightly doped epitaxial layer on a heavily doped substrate is a particularly useful material configuration for both reducing the bulk diffusion current and achieving a high generation lifetime in the vicinity of the surface.^{329-331,345} It has been noted that the benefits of IG as measured at room temperature, however, may be somewhat negated at device operating temperature due to the g-r current generated by the IG centers.²⁵⁹

Wafer Design

The incorporation of these strands into developing the optimal wafer was generically described as wafer design or defect engineering,¹²¹ the latter exemplified by Rozgonyi's famous *wheel of misfortune*³⁴⁶ and extended by Laszlo Fabry and colleagues (Fig. 26) as the *gear of challenge*.³⁴⁷ The recognition of the silicon wafer as an early version of the finished IC product, rather than a raw commodity material, has become more fully appreciated throughout the IC industry. This insight is used to guide the design of a circuit-focused, multizoned silicon wafer using a modular systems approach to improve the consistency and performance of IC products.¹²¹ By engineering the wafer specifications to achieve the variously configured multi-zone characteristics of silicon for the particular IC application, product performance, yield and reliability can be enhanced. While there may be no unique set of silicon wafer specifications applicable in all cases because of variations in both the IC fab processes and IC applications, an important cost-of-ownership (CoO) goal is to develop a sufficiently robust wafer and IC process in order to maintain cost control.

The multizone silicon wafer has been described and implemented by Howard Huff, ECS Fellow and Electronics Division 1996 Awardee in conjunction with Lawrence,^{101,121} and independently by Shin Takasu, and Hans Richter and colleagues.³⁴⁸⁻³⁵⁰ The structure consists of the circuit active zone (a), characterized by the requisite wafer surface flatness, metallics and localized light scatterers (LLS). This zone may be either the polished wafer surface or an epitaxial layer. The defect-free DZ region (b), is developed during the high-temperature thermal processes that accompanies the formation of the IG zone, region (c). Zone (c) getters the process-induced metallic contaminants (often responsible, in conjunction with structural de-



Figure 27. Harry Gatos (standing) and "his orchestra."

fects, for uncontrolled leakage currents) away from the circuit active zone during IC fabrication. The driving force for gettering is the reduction in the Gibbs free energy of the material system. The IG zone, however, generally exhibits an incubation time until it has sufficiently developed to form the getter complexes during IC fabrication. This incubation time is dependent on both the as-grown wafer characteristics and the detailed IC thermal process conditions, in conjunction with silicon interstitials, carbon and perhaps, dopants, resulting in the formation of IG centers. Recently, the formation of IG sites in the bulk gettering zone has been facilitated via engineering the vacancy concentration to enhance the clustering of oxygen, rather than focusing on the oxygen content per se (and the associated hi-lo-mod hi IG process) by Falster and colleagues.³⁵¹ The EG zone, region (d), is also a critical factor in the gettering process. This zone is generally active at the beginning of the IC fabrication process, whereas the conventionally formed IG zone, as noted above, requires a sequential set of process steps for its development. The back surface of the wafer, however, is increasingly being polished to reduce particle contamination, improve wafer flatness, and increase wafer strength. The polished back surface more readily exhibits microscopic contamination and wafer handling damage. As a result, back-surface cleanliness requirements may emerge and drive the need for more stringent robotic handler standards. Many EG techniques also degrade the quality of the polished back surface and the front-surface site flatness due to nonuniformities in the deposited back-surface gettering film and, consequently, may no longer be allowable.²²

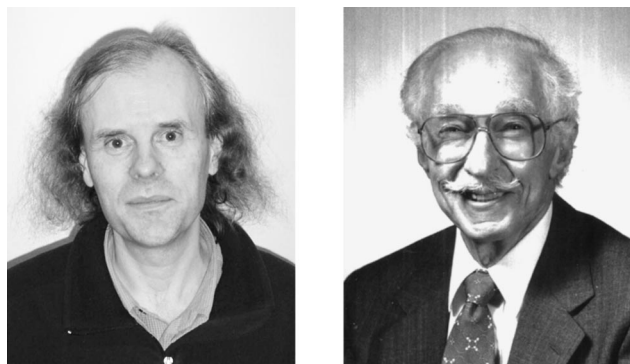


Figure 28. (left) Marc Heyns and (right) Bill Pliskin.



Figure 29. (left) Jerzy Ruzyllo and (right) Al Tasch.

Wafers with an epitaxial layer often incorporated an oxide seal zone (e), historically utilized in conjunction with external polysilicon (EG) gettering. The oxide back-seal has been utilized to prevent the transfer of silicon from the wafer to the susceptor in the case of front-surface radiant-heated epitaxial reactors and to minimize the autodoping phenomenon (substrate dopant transfer to the epitaxial layer of adjacent wafers by a complicated and variable time-dependent gaseous species transfer) as well as, presumably, the transfer of dopant to adjacent wafers during IC processing.³⁵² In some cases, an oxide-nitride seal zone or other composite films are preferred rather than the polysilicon-oxide configuration. The utilization of single wafer epitaxial reactors with both front- and appropriate back-surface heating lamps, however, has negated the silicon transfer effect while the autodoping effect during IC fabrication has been suggested, in retrospect, to not be that significant. In those cases where the back-surface oxide is still utilized during epitaxial deposition, the oxide is often subsequently removed per the IC customer's request. The oxide removal also significantly reduces the wafer bow. Accordingly, the back-surface oxide is no longer a recommended procedure for 300 mm p/p⁺ epitaxial wafers; indeed CoO considerations has been noted by Goodall and Huff to become especially important with the transition to the 300 mm wafer diam.^{22,353-355} Permutation of the multizone concept for variously configured zones or stacked layers leads to further specialized configurations.¹⁰¹

Surfaces and Wafer Cleaning

Although modern ICs are typically several cm² in spatial area and typically 0.75 mm thick (as fabricated), barely 1% by volume of the silicon material is required for the active device regions and interconnections. The surface structure and reactivity of silicon, including the importance of both wet and dry (plasma) cleaning methodologies, have therefore become of the utmost importance. Indeed, in recent years, the physical structure as well as the chemical nature of the wafer front surface has emerged as a critical concern. In the early days, preferential etchants were utilized for revealing defects such as dislocations in plastically deformed germanium as discussed by Gerald Pearson, 1981 ECS Solid State Science and Technology Awardee.³⁵⁶ A wide variety of wafer cleaning recipes were also developed, as exemplified by William Pliskin (Fig. 27), ECS Fellow and Electronics Division 1972 Awardee,³⁵⁷ Erhard Sirtl,³⁵⁸ and summarized by Harry Gatos (Fig. 28) and Mary Lavine.³⁵⁹ Cleaning the wafer surface was extended from these early studies to the current regime utilizing the SC1/SC2 methodology initiated by Kern²⁵¹ and subsequently expanded, taking into account both device performance and CoO implications. These studies included Marc Heyns (Fig. 27),³⁶⁰⁻³⁶² Tadahiro Ohmi,³⁶³⁻³⁶⁵ and Jerzy Ruzyllo (Fig. 29) ECS Fellow,^{366,367} and Richard Novak, co-editors of the ECS *Cleaning Technology in Semiconductor Device Manufacturing* proceedings and their colleagues. Takeshi Hattori has recently edited an

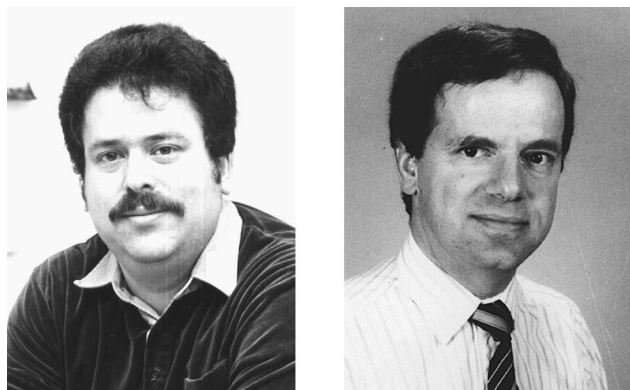


Figure 30. (left) Bernard Meyerson and (right) George Celler.

extensive monograph summarizing a number of cleaning technology and surface preparation processes and their relation to enhanced device performance.³⁶⁸ The preparation of the silicon surface, cleaning, passivation, and surface morphology, has played a significant role in ensuring the development of improved device performance and yield.

Both polished and epitaxial wafers exhibit specific defects that must be controlled. Polished wafer defects include metal and organic surface chemical residues, particles, and grown-in microdefects, such as COPs. Epitaxial wafer defects include large structural defects ($>1\ \mu\text{m}$), (such as epitaxial stacking faults¹⁹²) and small structural defects ($\leq 1\ \mu\text{m}$) as well as particles and residual chemical residues. Starting material requirements are expressed in terms of specific types of surface defects for different wafer types. The influence of the preoxidation clean on the SiO_2 growth rate, surface organics (apparently the carbon atom surface density) and its degrading effects on MOS GOI as well as the increased roughening of the silicon surface heated in a hydrogen ambient, compared to nearby surface regions covered with residual SiO_2 films, remain important arenas of research.¹ Indeed, the removal and prevention of surface defects is a current state-of-the-art challenge for silicon wafer technology with immense CoO implications. The development of laser scanning and other instrumentation to count, size, and determine the composition and morphology of these defects is a critical metrology challenge³⁶⁹ and continues to be addressed by a variety of equipment and fab personnel.

IC Scaling

Gordon Moore's assessment of memory component growth in 1965, initially based on bipolar and then MOS memory density, was observed to quadruple every 2 years²⁰ (modified to ~ 3 years around the mid-later 1970s and currently taken as 3-4 years based on a 1995 assessment²¹), became enshrined as Moore's law. Indeed, Moore's law became the productivity criterion by which the IC industry grew at a 25% compound annual growth rate (CAGR). Device scaling has been the engine driving this revolution, with major contributions arising due to reductions in gate dielectric thickness, physical gate length and extension junction depth, as discussed by Robert Dennard and colleagues via constant electric-field scaling and, subsequently, constant voltage scaling.^{370,371} These parameters were empirically related in 1980 by Simon Sze and colleagues;³⁷² Sze is the author of the influential textbook *Physics of Semiconductor Devices*.³⁷³ For example, consider the scaling of the KDRAM from the early 1970s (4K DRAM) to today's leadership MPU part appropriate for the 100 nm technology generation in 2003.²² The SiO_2 gate dielectric has proceeded from the range of 50-100 nm for the 4K DRAM to an anticipated value of about 1.2 nm oxide equivalent thickness (EOT) for the MPU part.²² Likewise, the physical gate length has decreased from 7.5 μm for the 4K DRAM to a physical gate length of about 45 nm for the MPU part at the 100 nm tech-

nology generation.²² Finally, the junction depth has decreased from several micrometers for the 4K DRAM to about 20 nm for the extension junction depth for the MPU part at the 100 nm technology generation.²² In a related fashion, the critical figure of merit for transistor speed, CV/I , has become less than one psec for an NMOS-FET and approaching one psec for a PMOSFET, as the physical gate length has decreased from 30 to 20 to 15 nm in leading edge research devices.³⁷⁴

Robert Dennard introduced the one-transistor memory cell in 1968,³⁷⁵ thereby establishing the paradigm by which enhanced scaling has progressed. Scaling of the gate dielectric SiO_2 to the sub-2 nm regime, however, has exacerbated the occurrence of direct tunneling^{376,377} as described by Yuan Taur and colleagues. An extensive global effort is in progress to identify an alternative, high-dielectric constant material to circumvent the gate dielectric direct tunneling leakage current in the case where the silicon oxynitride gate dielectric is less about 1.2 nm,^{22,378-382} including the relevant diagnostic techniques as described by Diebold and colleagues.^{19,383,384} Rajendra Singh, 1998 DS&T Callinan Awardee and co-editor of the ECS *Low and High Dielectric Constant Materials: Materials Science, Processing, and Reliability Issues* proceedings and the Materials Research Society's (MRS) March, 2002 issue of the MRS Bulletin, as well as other Symposia, continues the focus on alternative, high-k gate dielectric materials, gate electrodes (eventually requiring dual metal gates with differing work functions for CMOS optimization) and the issues of incorporating the gate stack into an integrated, conventional planar, initially poly electrode, IC process flow. Additionally, Al Tasch (Fig. 29), Electronics Division Awardee in 1997, has clarified the role of the quantum confinement effect in silicon in increasing the effective dielectric thickness of a MOSFET in inversion,³⁸⁵ which cannot be avoided as compared to the poly-depletion effect in the polysilicon gate electrode, which can be negated by utilizing metal gate electrodes. In that regard, a dual metal system with differing work functions is under consideration as the gate electrodes for optimal CMOS performance.²²

Concurrently, a host of studies are in progress to identify an ultrashallow junction fabrication methodology consonant with the sub-100 nm technology generations.^{22,386} These studies may be grouped under the classification as classical CMOS structures. On the other hand, a plethora of nonclassical CMOS devices are under consideration wherein a unique combination of materials and/or structural configuration of the device may differ from the conventional or classical planar CMOS structure.²² Of particular importance is the assessment of alternate channels for enhancement of the n- and p-channel mobility, ranging from strained silicon on unstrained Si-Ge on SOI, silicon-germanium on silicon and a host of alternative vertical transistor structural configurations^{387,388} as well as the ballistic transistor.³⁸⁹

Silicon-Germanium

The limitations of silicon electronic devices have warranted the development of compound semiconductors such as gallium arsenide with a larger electron and hole mobility as compared to silicon for specialized, mainly high frequency, electronic applications. The limited device integration possible with compound semiconductors, however, and the complexity of processing compound semiconductors has driven the extension of silicon technology by forming alloys of silicon with germanium as exemplified by Bernard Meyerson (Fig. 30), Electronics Division 1993 Awardee³⁹⁰⁻³⁹² and John Bean,³⁹³ and their colleagues as well as other research groups. The silicon energy gap ($E_g = 1.12\ \text{eV}$) at the X symmetry point can be monotonically decreased with the addition of germanium break ($E_g = 0.66\ \text{eV}$). The flexibility of tuning the energy gap in silicon-germanium alloys can improve the performance of specialized, high performance electronic devices.¹⁰³

In some cases, the germanium content is changed abruptly at a certain distance from the surface of the semiconductor to form an abrupt heterojunction, with a discontinuity in the energy gap. Because silicon and germanium have similar electron affinities, the



Figure 31. (left) Sorin Cristoloveanu and (right) Jim Meindl.

energy required to remove an electron from the bottom of the conduction band to outside the crystal, of 4.05 and 4.00 eV, respectively, the conduction-band edge is nearly continuous at the silicon-germanium boundary, while the valence band edge has a discontinuity large enough to modify device performance. This valence-band discontinuity is especially useful in bipolar transistors. The gain of an npn bipolar transistor is related to the ratio of the electron current injected across the emitter-base junction to the sum of the electron and hole currents crossing that junction. The valence-band discontinuity creates a barrier which decreases the injection of holes from the base into the emitter, thereby increasing the gain of the transistor. A further approach to improving bipolar transistor performance is accomplished by increasing the germanium content gradually with position in the base layer. In this case, the energy gap varies as a function of position across the base region of the transistor. The varying energy gap creates an internal electric field which accelerates the free carriers (*i.e.*, electrons in the case of an npn transistor) across the base region, thereby increasing the maximum frequency response, f_t , of the bipolar transistor towards 100 GHz.

A p-channel silicon MOS transistor has a small hole mobility. The hole mobility in silicon-germanium alloys, however, can be greater than in pure silicon.³⁹³ The increased carrier mobility enhances the transconductance of the p-channel MOS transistor. Furthermore, in silicon-germanium p-channel MOS transistors a thin layer of silicon-germanium, slightly separated from the oxide-semiconductor interface by a silicon layer, can spatially confine holes. These confined holes travel in the silicon-germanium layer and, accordingly, their velocity is not reduced by scattering from the oxide-semiconductor interface.

Optimal electrical properties were achieved by ensuring the crystal bonding is uninterrupted across the silicon/silicon-germanium interface. The lattice constant of germanium, however, is $\sim 4\%$ greater than that of silicon. The lattice mismatch increases with increasing germanium content in silicon-germanium alloys. Modern growth techniques using CVD can form a thin layer of silicon-germanium alloy on silicon with a continuous crystal structure across the interface (*i.e.*, the crystal structure is commensurate). The alloy layer, however, is compressed in the plane of the film. With increasing layer thickness, the energy associated with compressing the alloy layer to fit the silicon crystal increases. Above a critical thickness,³⁹⁴ the strain energy exceeds the energy necessary to form misfit dislocations. As the bonds across the interface break to form the misfit dislocations, the strain in the system is reduced, thereby lowering the total energy. Accordingly, although silicon-germanium layers thicker than the equilibrium critical thickness can be formed, they are unstable.³⁹⁴ When these metastable layers are heated above the stability temperature appropriate to the layer thickness and germanium content, any irregularity already present can nucleate a misfit dislocation, taking into account kinetic considerations. The dislocation then propagates along the interface, creating a line of broken



Figure 32. (left) Don Shaw and (right) Jerry Woodall.

bonds. While misfit dislocations at the interface may be detrimental to device performance, interactions between misfit dislocations may more seriously degrade the electrical performance of devices built in the layer. The limited stable thickness of silicon-germanium, therefore, constrains the application of silicon-germanium layers. Because very high-performance devices require thin layers (<100 nm) to limit carrier transit times, however, this restriction is not serious. Thin silicon-germanium layers are indeed compatible with device requirements.

The strain in silicon-germanium layers also exhibits the beneficial effect of increasing the energy gap difference relative to pure silicon.³⁹⁵ For example, while an unstrained silicon-germanium layer containing 20% germanium has an energy gap about 0.09 eV smaller than that of silicon, the energy gap of a strained layer with the same germanium content is about 0.17 eV smaller than that of silicon. The required electrical performance can, therefore, be obtained with a smaller germanium content in a strained, rather than an unstrained, layer.

Carrier mobilities in silicon-germanium layers are expected to differ from the silicon values for several reasons. First, carrier mobilities in germanium are greater than for silicon. Second, the random arrangement of germanium in the silicon crystal structure leads to a reduction in mobility due to an additional scattering mechanism, referred to as alloy scattering. Third, the strain in the silicon-germanium layer modifies the curvature of the energy bands, changing the carrier effective mass and, thereby, the carrier mobility. Finally, the carrier lifetime is strongly reduced due to impurities such as oxygen in the film. Because oxygen is more readily incorporated into silicon-germanium alloys than in silicon, a higher purity ambient is required when forming silicon-germanium alloys compared to elemental silicon films. While most applications of silicon-germanium focus on high-performance transistors, optical devices

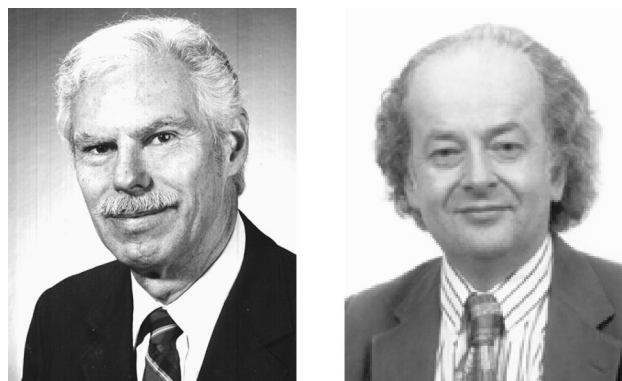


Figure 33. (left) Glenn Cullen and (right) Federico Capasso.



Figure 34. Microelectronics Revolutionaries. The 1998 Silicon Symposium celebrated the 50th Anniversary of the commercialization of the point-contact transistor, and included a special historical session, “Fifty Years and Counting”. Presenters included: (front row, left to right) Norman G. Einspruch, Yoshio Nishi, Bruce E. Deal, S. M. Hu, Junichi Nishizawa, R. C. Newman, and George Rozgonyi; (back row, left to right) Ulrich Gosele, Alfred Seeger, Else Kooi, Jack S. Kilby, Howard R. Huff (Helen Huff, who provided secretarial assistance), Takao Abe, Michael Riordan, Hans J. Queisser, Kurt Hubner, Kiyoo Itoh, and Hideki Tsuya.

may also become important.³⁹³ Because the energy gap of silicon-germanium alloys is smaller than for silicon, the optical absorption edge corresponds to a longer wavelength (*i.e.*, smaller energy) and silicon-germanium is useful as a photodetector at longer wavelengths compared to silicon.

Silicon-on-Insulator

Silicon-on-insulator (SOI) offers the potential for high speed, low-power consumption, soft-error and latch-up immunity, manufacturing process simplification, and smaller chip size. Current SOI manufacturing techniques result in wafers that are more costly than polished or epitaxial wafers. Nevertheless, the benefits often outweigh the higher wafer cost. Some bulk IC designs may be transferred directly to SOI substrates. However, optimization frequently requires mask set and process sequence modifications. In any case, the broad variety of today’s IC applications such as MPU’s, servers, smart power, RF signal processors require a considerable range of Si-device layer and buried oxide (BOX) layer thicknesses. A number of SOI wafer fabrication approaches are more fully entering into production to serve this range of SOI applications. In that regard, Harold Manasevit, who received the 1975 Electronics Division Award for his research on the chemical vapor deposition of silicon-on-sapphire (SOS), Katsutoshi Izumi, who introduced the SOI concept in 1988,³⁹⁶ Jean-Pierre Collinge,³⁹⁷ P. K. Vasudev,^{398,399} and George Celler (Fig. 30), ECS Fellow and Electronics Division 1994 Awardee^{400,401} including their colleagues have been long-term proponents of the eventual benefits and utilization of SOI, as has Sorin Cristoloveanu (Fig. 31), the 2002 Electronics Division Awardee and co-editor of the ECS *Silicon-on-Insulator Technology and Devices* proceedings, and his colleagues, who introduced the first double-

gate MOSFET in SOI in 1988.⁴⁰²⁻⁴⁰⁴ James Meindl (Fig. 31) has suggested that the double-gate MOSFET with intrinsically doped silicon⁴⁰⁵ may indeed be a potential candidate for the end-of-the-roadmap device structure.

Structural and defect characterization of the various SOI wafer fabrication techniques (*i.e.*, bonded, implanted . . .) and correlation among the SOI properties, device characteristics and yield continues to be essential. The relative immaturity of SOI materials compared to polished and epitaxial wafers leads to an additional challenge for the understanding of SOI-specific defects and their impact on device performance and yield in a production environment.

Metrology for SOI wafers is a significant challenge. The particle and site flatness general metrology ITRS characteristics for polished and epitaxial wafers are not applicable for SOI wafers. This arises because interference effects arising from multiple reflections from the Si and BOX layers fundamentally alter the response of optical metrology tools compared to polished and epitaxial wafers, generally degrading the particle measurement capability. The anticipated shift from capacitive to optical measurement of wafer site flatness beyond the 100 nm node may cause a similar degradation of site flatness measurement capability. Metrology methods for many of the SOI defect categories call for destructive chemical etching that decorate but do not uniquely distinguish various types of crystal defects. These defects may not all have the same origin, size, or impact on the device yield, and therefore may exhibit different electrical effects on device characteristics. Nondestructive and fast-turn around methods are needed for the measurement of electrical properties and structural defects in SOI materials.

Nanoelectronics and Compound Semiconductors

The fabrication of artificially structured multielement composites has created new and fascinating devices which may yield the "transistor of the 21st century." These quantum-based devices may be fabricated in multi-layered heteroepitaxial crystalline, disordered or amorphous III-V compounds and more complicated alloys, which may include crystalline or amorphous silicon and silicides.^{101,103} The characteristic dimension of these structures perpendicular to the multilayers is comparable to the wavelength of the carrier transport species, resulting in unique optoelectronic quantum properties. Significant contributions to this arena have been made by a number of outstanding personnel, including ECS Fellows Ben Streetman and Jun-ichi Nishizawa (Fig. 34). Jerry Woodall (Fig. 32), ECS President in 1990-1991, Solid State Science and Technology 1985 Awardee and Electronics Division 1980 Awardee,^{406,407} Nick Holonyak, co-author of *Physical Properties of Semiconductors*, in conjunction with Charles Wolfe, Electronics Division 1978 Awardee and Gregory Stillman,⁴⁰⁸ Alfred Cho, Solid State Science and Technology 1987 Medalist and Electronics Division 1977 Awardee who established the utilization of molecular beam epitaxy (MBE) for compound semiconductor device fabrication, Morton Panish, Solid State Science and Technology 1979 Awardee and Electronics Division 1972 Awardee,⁴⁰⁷ Don Shaw (Fig. 32), Electronics Division 1983 Awardee,⁴⁰⁹ Glenn Cullen (Fig. 33), ECS Fellow and Electronics Division 1982 Awardee,^{410,411} Bertram Schwartz, Electronics Division 1987 Awardee, S.N. (George) Chu, ECS Fellow and Electronics Division 2000 Awardee, D. Noel Buckley, ECS Fellow and Stephen Pearton, ECS Fellow and their colleagues have played immense roles in the development of these endeavors. The fabrication of artificially structured semiconductors, including the quantum cascade laser, are being developed by Federico Capasso (Fig. 33) and colleagues. They are shaping energy band diagrams to design quantum-structured material configurations to achieve unique device phenomena and characteristics.⁴¹²⁻⁴¹⁴ In that regard, Herbert Kroemer has played a most significant role in the science and technology of heterostructures and their applications.

One consequence of this shrinkage of vertical dimensions is the confinement of electrons to such an extent that they no longer exhibit a vertical degree of freedom. The electrons become a two-dimensional electron gas exhibiting very high electron mobilities at low temperatures and unique characteristics. Effects heretofore studied only in basic research projects are becoming realistically achievable and have been discussed, for example, by David Lockwood, ECS Fellow and co-editor of the *ECS Quantum Confinement: Nanostructured Materials and Devices* proceedings, and colleagues. Indeed, spintronics and single electron devices, for example, may offer significant opportunities. One must be cautious, however, to critically assess technological proposals as regards their applicability for both room-temperature operation and for commercial large-scale integration, although selected niche technologies should also be explored.

Quantum interference effects of much larger magnitude are seen even above room temperature in tunneling devices, which operate far from equilibrium. Resonant tunneling diodes exhibit sharp peaks in tunneling current due to the resonant transmission of electrons through quantum well states. Transistors based on this phenomenon have been demonstrated and they may well form the basis for a new scalable IC technology such as the tunneling-based static random access memory (TSRAM) based on the integration of resonant tunneling diodes with heterostructure field-effect transistors providing for fast digital processors with the required large amounts of fast memory "on chip."⁴¹⁵

Forever Silicon?

The dominant material in the industrial revolution, after more than a century of high volume production, continues to be steel.⁴¹⁶ It was only in the 1920s, however, that the fundamental physical chemistry of steel became firmly understood in terms of its thermodynamic and kinetic properties. At this stage, it appears that we are

at a similar stage in the development of our understanding of silicon materials technology. Although crystalline silicon and silicon-based material systems such as Si-Ge have been extensively studied, a thorough description of its material properties is precluded at present due to its extreme structure-sensitivity. The opportunities for further silicon-based IC advancements, including non-planar configurations of silicon ICs, appear boundless, certainly quite sufficient to support numerous research and development thrusts well into the 21st century. Other structural materials, such as Al and plastics, have, of course, entered the mainstream based on their strength-to-weight ratio for structural materials.⁴¹⁶ Similarly, one must be cognizant of paradigm shifts to other material systems for microelectronics, based on the power-delay product, for example, as a useful figure of merit in assessing opportunities for gigascale integration. James Meindl has carefully explicated the trends and fundamental limitations from a systematic analysis for silicon materials, devices, circuits and systems⁴¹⁷ as well as clarify the role of interconnection limitations.⁴¹⁸

Adventurous technological proposals, however, must be critically assessed as regards their applicability.⁴¹⁹ That is, it is essential to not only understand new technologies, but to also comprehend its impact on the future market structure. Accordingly, development of silicon-based opto-electronic systems utilizing porous silicon or alternative quantum-well structures, quantum dots, single-electron devices and other mesoscopic material systems should be carefully assessed as regards their capability of room-temperature operation and applicability for commercial large scale integration applications. Nevertheless, the fabrication of amorphous silicon is an arena of intensive research, affording significant insight into neural networks and thus, perhaps, artificial intelligence. Microclusters, small aggregates of atoms constituting a distinct phase of matter or immersed in a higher-dimensional matrix, may offer unique applications not fully anticipated, especially for a fully integrated silicon optoelectronic system. Additionally, the crafting of molecules and small chemical groups into transistors and related components of computer chips and the appropriate wiring connections has been accelerating. Organic and biological molecules have been identified which can be photochemically "switched" in less than 1 psec, comparable to the fastest inorganic semiconductor electronic devices. Indeed, Langmuir-Blodgett organic films or self-assembled monolayers may also be useful in future electronic applications. Furthermore, merging the self-assembly of biological materials with a variety of properties of inorganic compounds (*i.e.*, electronic, magnetic and structural) to develop nanoparticles into macrosized structures has piqued the interest of a number of research and engineering groups.

The drive for efficient photon emission from silicon to develop a low cost silicon-based optoelectronic integrated system has been continuing. The recent compatibility of optically active compound semiconductor materials, such as GaAs, structurally commensurate with silicon materials through engineered interface configurations, may accelerate the fabrication of an optoelectronic system compatible with silicon technology.⁴²⁰ This combination of gallium arsenide with silicon may be especially important inasmuch as the potential benefit of gallium-arsenide due to its electron mobility of 8500 cm²/V s has previously been noted to be limited as a result of the thermally limited switching time as well as ULSI system-level limitations such as interconnection resistance.⁴²¹ Finally, the development of optical interconnections for a micro-phonic technology would be of immense importance to facilitate the achievement of GHz clock speeds.

Studies in various degrees of research and development including cellular automata, self-assembled structures, fullerenes, carbon nanotubes, metallic clusters in dielectrics and the role of reduced dimensionality in these structures, high-temperature superconductors, optical computers, quantum computers, DNA computers, and other arenas not comprehended as yet, represent areas where major research and selected applications may evolve. In that regard, Carver Mead, 1971 DS&T Callinan Awardee co-author of the widely utilized textbook, *Introduction to VLSI Systems*,⁴²² may offer

some guidance during his plenary address at the Centennial Meeting of The Electrochemical Society in May, 2002. Indeed, it will be interesting to read the Electronics Division review in 2052!

The phenomenal growth of the IC industry, achieved by staying on the "productivity learning curve," continues to be the gauge by which the industry is measured.^{20,22} This is evidenced by the cost per bit or logic function historically declining at ~25-30% CAGR for nearly the past three decades. This growth has been fueled by four factors; shrinking lithographic design rules, yield improvements, increased equipment utilization, and larger wafer diameter. The largest opportunity growth factor to maintain the IC productivity engine and continue on the productivity curve as described by Moore's law^{20,21} appears to be increased equipment effectiveness; that is, the percentage of time the equipment is adding value to the wafer. The largest challenge to maintaining the productivity curve, however, may be the enormous financial infrastructure required, rather than technological limits to chip density. In that regard, business and manufacturing ideas will become increasingly important to ensure that the long-term productivity growth of the semiconductor industry maintains its growth near historical levels for the next ten years. More than just monitoring productivity, whether by staying on the productivity curve or increasing manufacturing effectiveness, however, is required. Rather, modeling productivity, the identification of new productivity measures, is required.⁴²³ Global specifications, metrology and standards, in addition to CoO opportunities as discussed earlier, are important mechanisms to ensure the marketplace reality of the ITRS roadmap trends, based on Moore's law, is achieved. The cost effectiveness of international standards for emerging technologies such as SOI and 300 mm diam wafers, in conjunction with the cost-effective production of ICs, such as computer-based design for manufacturability, will offer significant opportunities for an improved quality of life for the world's citizens.

Accordingly, silicon MOSFETs may be expected to scale in an essentially predictable manner from the present state-of-the-art 100 nm technology generation (physical gate length of 45 nm) to the 22 nm technology generation (physical gate length of 9 nm).²² Nevertheless, the IC industry has continually seen that the ingenuity of device and process engineers to develop unique device geometries, from the early DRAM era⁴²⁴ and, more recently, nonclassical CMOS devices including vertical transistor configurations utilizing SOI in some cases, double-gate structures with SOI, novel process technologies and models to guide further development may be more influential on IC growth and device performance than might be inferred from extrapolation of today's art and may offer significant unforeseen opportunities.⁴²⁵⁻⁴²⁷ The ubiquitous applicability of Si technology in the information revolution, touching numerous aspects of the lives of the worlds' citizens, however, may not necessarily require the state-of-the-art technologies in all applications. It is unlikely, however, that the present worldwide silicon infrastructure will be regenerated to support a silicon successor.⁴²⁸ Accordingly, silicon technology is expected to continue as the most powerful driver of the information age for at least the next 100 years.

Acknowledgments

This review is dedicated to the memory of Dr. Else Kooi (1932-2001). Discussions with Takao Abe, Kenneth Benson, Werner Berg-holz, W. Murray Bullis, Randal K. Goodall, L. C. Kimerling, Bernd Kolbesen, George A. Rozgonyi, Walter R. Runyan, Dieter K. Schroder, Fumio Shimura, Shin Takasu, Hideki Tsuya, and Masaharu Watanabe have been and continue to be a source of insight and stimulation. The author appreciates Cor Claeys, chair of the Electronics Division of The Electrochemical Society and Paul Kohl, Editor of the *Journal of The Electrochemical Society and Electrochemical and Solid-State Letters* affording the author the opportunity to prepare this review. Finally, we wish to thank all of those who provided the photographs used throughout the article as well as those whose photographs, unfortunately, did not arrive in time for inclusion.

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